RD50-MPW2 C-V Measurements on test matrices at IFIC

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RD50-MPW2 C-V measurements: setup



Keithley 237

source meter

WAYNE KERR

(measure

Capacity)



- Setup inside a black box in the clean room.





- GND, 8 surrounding pixels and central pixel pads connected together to GND.

- HV pad and chuck connected together to HV.

RD50 HV-CMOS Meeting

Capacitance calibration

- Measure the capacitance with the 4 needles connected but without touching the pads: C \approx 1.2 pF
- Once we do the measurements, extract the parasitic capacitance (parallel) and divide by 9 (9
 pixels connected in parallel).



RD50 HV-CMOS Meeting

• C-V Measurements W8_2(0.5-1.1 k Ω cm) every geometry:



• C-V Measurements W7_4(0.5-1.1 k Ω cm) every geometry:



• C-V Measurements W11_4 (1.9 k Ω cm) every geometry:



• C-V Measurements W10_2(1.9 kΩcm) every geometry:



• C-V Measurements W14_3(> 2 k Ω cm) every geometry:



• C-V Measurements W13_4 (> 2 k Ω cm) every geometry:



• C-V Measurements 1st matrix (rounded, 3 µm spacing):



• C-V Measurements 2nd matrix (rounded, 8 µm spacing):



11

• C-V Measurements 3rd matrix (chamfered, 8 µm spacing):



12

• C-V Measurements 4th matrix (squared, 8 µm spacing):





- Capacitance between 100 125 fF for each pixel.
- MPW2 Documentation: "According to schematic simulations with Cadence, parasitic capacitance of one pixel is less than 200 fF when SUB is at -60 V."
- The shape of the C-V curve is the one expected.
- Looking at the C-V curve shape, we can confirm that the pixel is mostly depleted at -10 V.