MOSAIC (MOdular System for Acquisition Interface and Control)

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List of topics:

• Hardware description and functionality (available by June)
  – Number and type of I/Os, bandwidth, powering…
  – Interface to PC/DAQ system, in particular for integration in beam telescopes
• Planned/possible hardware updates and respective timeframes
• Production and distribution
  – Possibility to produce, commission and distribute ~20 systems by June
  – Unit cost
• Institutes responsible and manpower available
  – For design and production of proximity/carrier cards
  – For firmware development and maintenance
  – For software development, including integration in DAQ frameworks (e.g. EUDAQ)
  – Involvement after MLR1 - in ER1 and full-scale prototypes
• Application examples
Hardware description and functionality

- VME board (only for power supply)
  - Requirements: +5V 2A, -12V for NIM
- 10 Hi speed Input + 10 Hi speed output Up to 6.6 Gb/s
- 2 x 33 general purpose LVDS I/O (~1Gb/s)
- 2 expansion slots – FMC Mezzanine boards
- 4 NIM configurable I/O
- 1 DDR3 – SODIMM connector with 1GB module
- Gigabit Ethernet interface
- Xilinx FPGA: XC7A200T-2 FFG1156C
Hi speed connector & cable

- 24 differential pairs for each cable (12 for side)
- 2 Cable for connector (**1 Unused**)
- Compact assembly (28 mm x 32 mm with shield)
- Standard cable length:
  - 1 m -> 6.44 GHz bandwidth
  - 2m -> 2.56 GHz bandwidth
- Signals
  - 10 Hi speed TX
  - 10 Hi speed RX
  - 2 LVDS Clock
  - 2 MLVDS Control
Firmware – ALPIDE TB

- Control & Monitor protocol: UDP
- Transfer rate to DDR3 memory: 6 GByte/s
- DAQ protocol: TCP
- Sustained transfer rate: 120 MByte/s
- IP address configurable
- Firmware upgrade via Ethernet

FPGA resources utilization
“Collaborative” mode

Many boards can be connected in a Master-Slave mode

Master distributes clock, trigger, sync and pulse to slaves

If only one slave, only two NIM cables are needed
Available Software

C++ library:
• Base classes to access blocks mapped on WishboneBus
  • Generic control protocols: I2c, SPI, ALPIDE
• Generic Data acquisition base class
  • ALPIDE
  • VFAT3
  • FATIC
• Run and trigger control class

Some acquisition and test software already developed
Possible hardware updates: FMC slot

- 2 FPGA Mezzanine Card (FMC) Low Pin Count or 1 Double Width Card
  - 34 diff pairs lines or 68 single ended => User defined
  - 2 diff clock lines => Clock
  - 1 Bidirectional High speed transceiver (up to 6.6 Gbps)

- Conform to the VITA Standard ANSI/VITA 57.1
12 channel ADC card

FMC112 FPGA Mezzanine Card

- 12-channel ADC 14-bit 125 MSps
- Manufacturer provides “Board Support Package” including RTL source code
- Fast firmware integration (2-3 Weeks from hardware receive)

SMA breakout adapter
From 2015 to now we produced 90 Boards distributed to many labs around the word. Can some of them be reused?

Costs
MOSAIC Board: ~2500 Euro
FMC112 ADC Board: 4000-5000 USD (Depending on quantity and configuration)

Delivery
MOSAIC Board: 8 weeks from order
FMC112: 10 - 12 weeks from order
Institutes responsible and manpower

For design and production of proximity/carrier cards:
Limited resources available in Bari, preliminary interest expressed by other INFN groups

For firmware development and maintenance:
INFN Bari (Giuseppe De Robertis)

For software development, including integration in DAQ frameworks (e.g. EUDAQ):
Some resource available, but additional contributions are welcome

Involvement after MLR1 - in ER1 and full-scale prototypes:
YES – MOSAIC is tailor-made for reading full-sized chips and small to medium-sized systems
Application examples:
ALPIDE single chip
Application examples: ALPIDE telescope

9 ALPIDE chip on carrier board
1 IB like mother board
1 Adapter FireFly to EyeSpeed

Cutesy of Andry Rakotozafindrabe
CEA Saclay
Application examples: ALICE MFT test beam

In theory:

- 30 ALPIDE chips on 3 ladders
- 3 MOSAIC boards

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Application examples:
ALICE ITS Test Setup - Endurance

<table>
<thead>
<tr>
<th>2</th>
<th>MOSAIC Boards</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>High Speed link</td>
</tr>
<tr>
<td>20</td>
<td>Control interfaces</td>
</tr>
<tr>
<td>1</td>
<td>I2C interface</td>
</tr>
<tr>
<td>10</td>
<td>Modules under test</td>
</tr>
<tr>
<td>140</td>
<td>ALPIDE chips</td>
</tr>
<tr>
<td>73.4 Million</td>
<td>Million of channels</td>
</tr>
</tbody>
</table>
CMS-VFAT3 characterization setup
VFAT3 Production test

ZIF Socket
Thanks