RD51 Collaboration

ECFA Detector R&D Roadmap Symposium Task Force 1 Gaseous Detectors 29 Apr. 2021

Electronics for MPGDs

front-end and DAQ for gaseous detectors R&D

Requirements electronics charge readout MPGD	2-6
Motivation for SRS readout system	7-12
VMM frontend	13-15
SRS DAQ systems	16-22
New DAQ architectures with SRSe	23-24
Collaborations,Testbeam pilot systems	25,26
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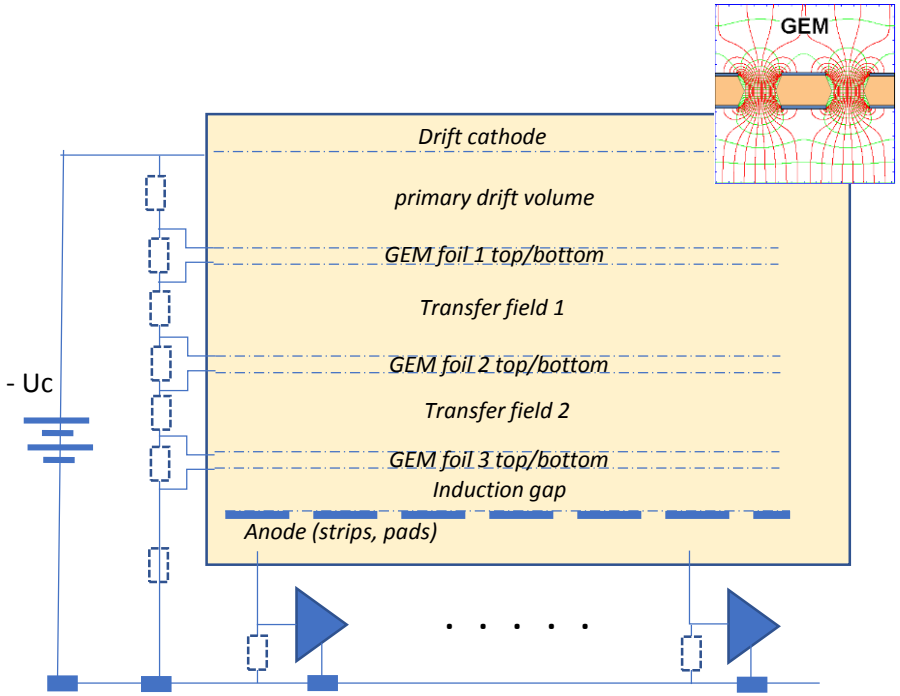
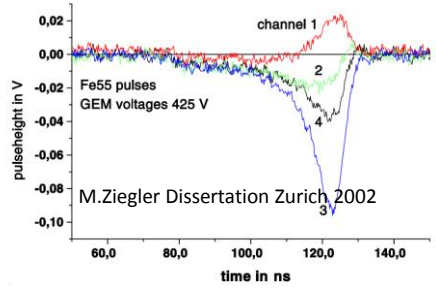
GEMs

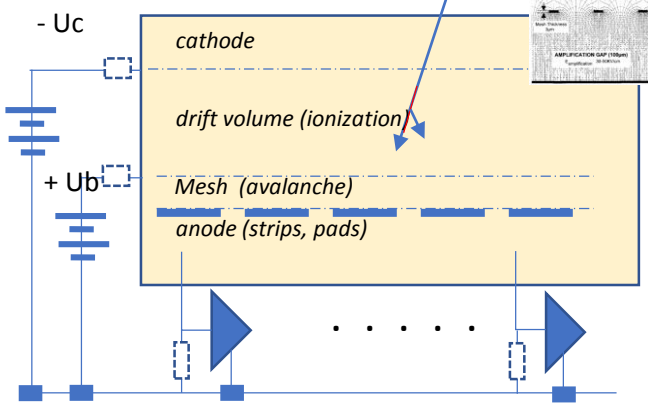


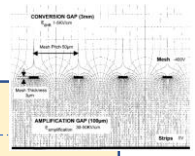


-separation e-/ions in successive (3-4) stages lower gain
-electron-peak pronounced but O(20 ns)
-ion tail induced by field frame

MicroMegas

Drift-sourced y, e-

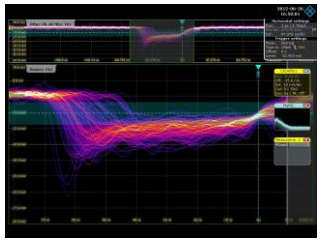




primary ionization in MPGD drift field neutral gas ($ArCO_2$)
- charge multiplication in micromesh field

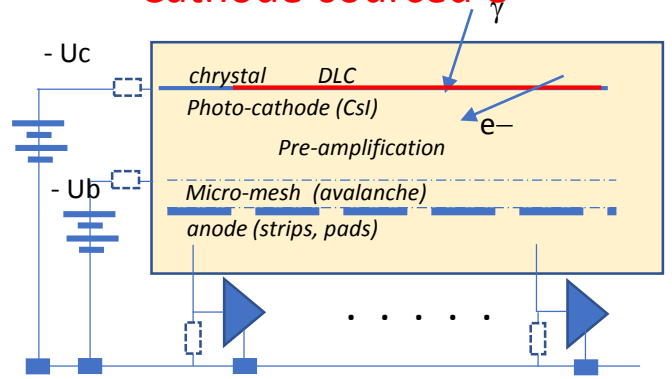
➔ **timing O(10ns)**

- [drift variation of 1st e- cluster arriving at mesh]



4GHz amplifer MM strip
Lab Oscilloscope MM y source ^{90}Sr H.Muller 2012

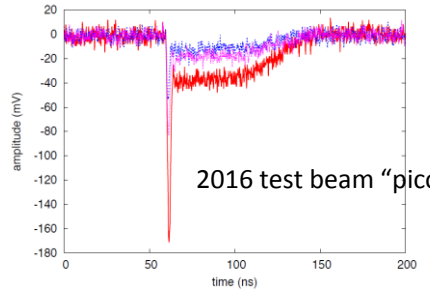
Cathode-sourced e-



- primary electron from photo cathode
- special gases (flammable)
- charge multiplication in micromesh field

➔ **timing O(10psec)**

- [jitter of cathodic electrons]



2016 test beam "picosec" signal

Hans.Muller@cern.ch

avalanche charge signals

detector capacity C_{det}

short connection to short single detector strip/pad: 20pf – 100pF
long strips, traces , cables : up 1nF
-> typ. ENC noise levels **1000e- @ 50pF**, min 400e- up 10.000 e-

input charge:

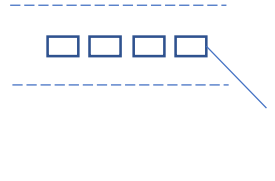
gas gain 1000 …10.000 , primary gas ionization 1…10 ->min 1000 e- (0.16 fC),
typical O(**1fC)** , up to 100.000 e- (16 fC)

signal shape MM

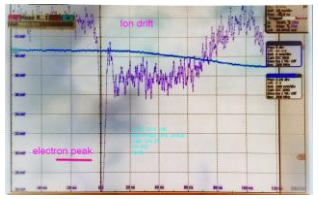
very fast avalanche (neg) electron peak (**tr < 1ns**) followed by slow ion tail **20..50ns**
capacitive coupling to enhance timing. Positive induced signals on neighbor strips

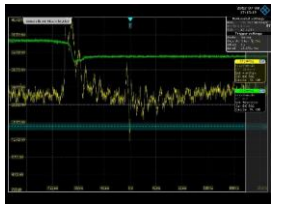
sparks and protection

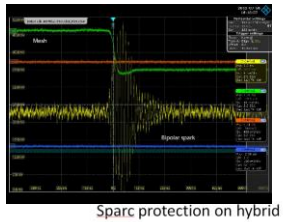
statistically unavoidable spark energy $\boldsymbol{E} = \frac{\mathbf{1}}{\mathbf{2}}\mathrm{CU}^2$ instanteneous very high dI/dt
-> protection circuits (TVS diodes) combined w. lowest impedance to detector GND
to minimize any inductive Voltage.
AC coupling to prevent galvanic destruction & enhance signal risetime over ion tail

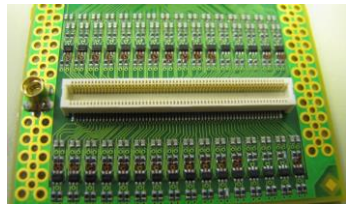


anode striplines 10cm
2mm gap 0.4 mm
min 15 pF
add connector, traces, etc
Cdet min. 20pF typ 50pF



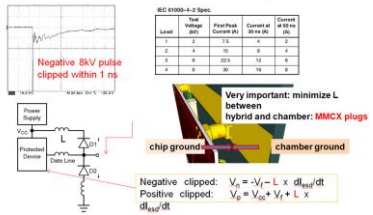






Sparc protection on hybrid

NUP4114UPXV6 quad ESD diodes: < 1 pF



ASIC-internal signal conversion

Charge pre-amplifers:

CSA type, convert charge to voltage
input capacity high @ low input impedance: insensitive to sparks
max . Gain is technology dependent [Cf] **16 mV/fC.. 0.5mV/fC**

noise:

ENC = f(Cdet, preamp technology & gain, shaping time)
main variable is Cdet. Aim for **1000 e- @ 50 pF**

dynamic range:

Assume min. gain 0.5mV/fC & Vcc =1.2V : max amplitude 0.9 Vcc
(0.9 * 1.2) / 0.0005 = 2160 fC (2 pC)
Assume ADC resolution 1mV, max 1024 mV -> **1024 (10 bit)**

shapers and peaking times:

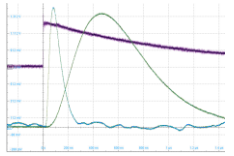
bandpass filter to suppress noise from signal carrier band
semi-gaussian peak amplitudes proportional input charge
noise minimum-relation between Cd and shaping time.
peaking times 25ns -400ns to match Cd of given detectors

pileup cancellation , high rates:

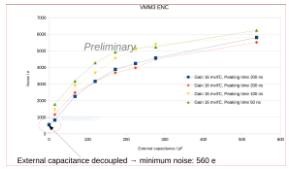
reset preamps at shaper peak (=> cancel preamp tails)
challenging technology (pole-Z obsolescence **). Channel rates up 4 MHz**

peakfinder ADC:

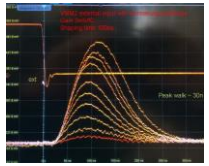
peak of semigaussian shaper=primary charge information
10 bit (match dyn. range), low deadtime, low noise
Aim: 10b @ 100ns or better



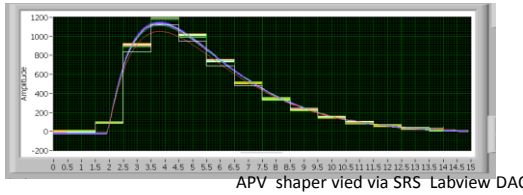
ASIC internal: CSA preamplifier fast signal step withslow discharge
Followed by gaussian-like shaped signal



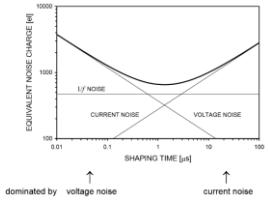
VMM3a Noise measurements VMM3 M.Lupberger, H.Muller 2018
revised by *Emorfili Terzimpasoglou* Miniweek Feb 2021



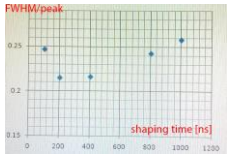
VMM : DDF shaper and noise
IEEE Trans. Nucl. Sci Vol.60 ,
No3 June 2013



APV shaper vied via SRS Labview DAQ
S.Martoiu



tutorials H. Spieler



Small GEM : noise measured with
^{55}Fe spectrum versus shaping time
Summer student project GDD lab

Feedback Preamp with charge injection
BNL: FE ASIC Lar TPC & VMM ATLAS)

ADC technology for 130 nm ASICs
SAR: 50 MS/s, 1 mW, 10 bit (Rivetti TF7)
Clockless CMD 10bit @ 250ns (BNL: FE ASIC Lar TPC & VMM ATLAS)

Trigger, timing and space resolution

Level-0 trigger:

option A for detectors with external trigger (GEM Telescopes, mesh-triggered MMs)
trigger latency: ASIC-internal **pipelines min. 1us, better 10 us**
Zero suppression for high rates

triggerless readout:

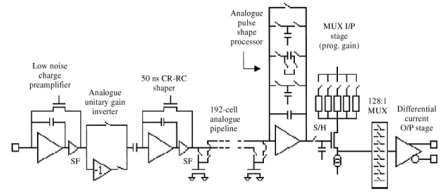
option B for high-rate data streaming, based on threshold only. Allows for
external long latency data pipelines (TPC's)
data links min.10M hits/s better 20 Mhit/s (32 bit encoded hit frames **~ 800 Mbps**)
Z-suppression hardware mandatory.

cluster logic:

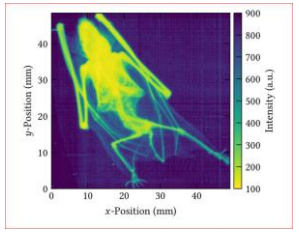
cluster detection with neighboring channels incl. edge channels < threshold
(improved space and energy resolution)

TDC for timing:

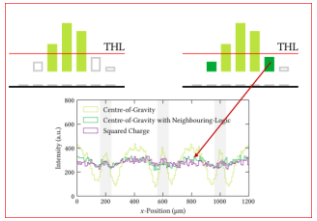
time measurement relative to clock: ToT, threshold, peak.
combined with **amplitude-invariant shaper**, target for O(50 ps): with 40 MHz clock
25/0.05 ~512 -> **9 bit TDC**



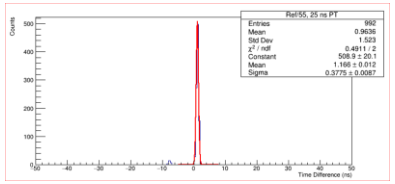
APV 25 ASIC: 192 deep analogue pipeline



Data driven (VMM3a SRS) readout of
277 Million clusters in 3 minutes
L. Scharenberg WG5.1 User meeting 26.04.21



L. Scharenberg GDD meeting 18.11.2020



prelim. 1.1 ns with VMM readout SRS
L.Scharenberg, "Time resolution of the VMM3a in the SRS"

Links for **D**ata, **T**rigger, **C**lock, **C**ontrols (DTCC)

Data and event-Flag uplinks:

2x 800 Mbps

8b10b encoded LVDS shielded twisted pair

configuration bitfile download:

ASIC Flash FPGA (1 x 400 Mbps)

8b10b encoded LVDS shielded twisted pair

Registers R/W:

FPGA, Sensors, ADC's, DACs..

I2C over twisted pair 100 kbps

Clock downlink:

optionally encoded trigger

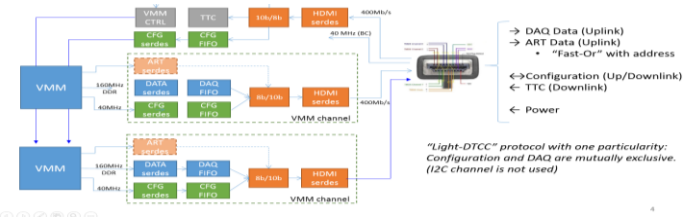
40 MHz typical, LVDS shielded twisted pair

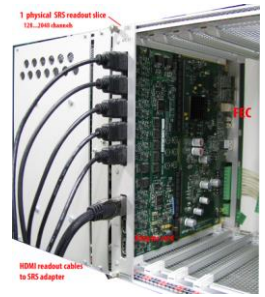
Power (optional over HDMI)

low-power ASICS (APV ..)

Mower monitoring on backend

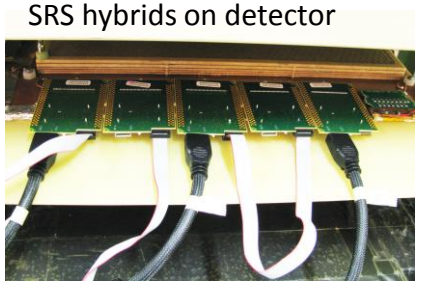
HDMI cables* chosen as DTCC frontend links for SRS in 2009



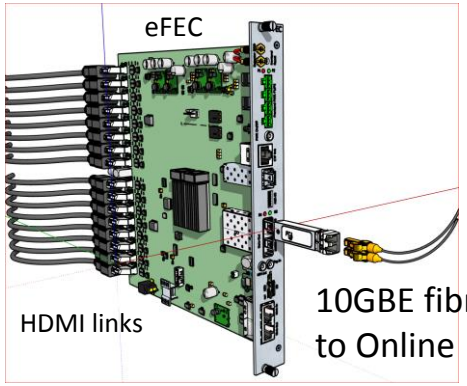


More: https://drive.google.com/file/d/1BxfOH5a2E9bxuWXv16IQsqRTNGpzuwHG/view?usp=sharing

SRS hybrids on detector



HDMI readout links

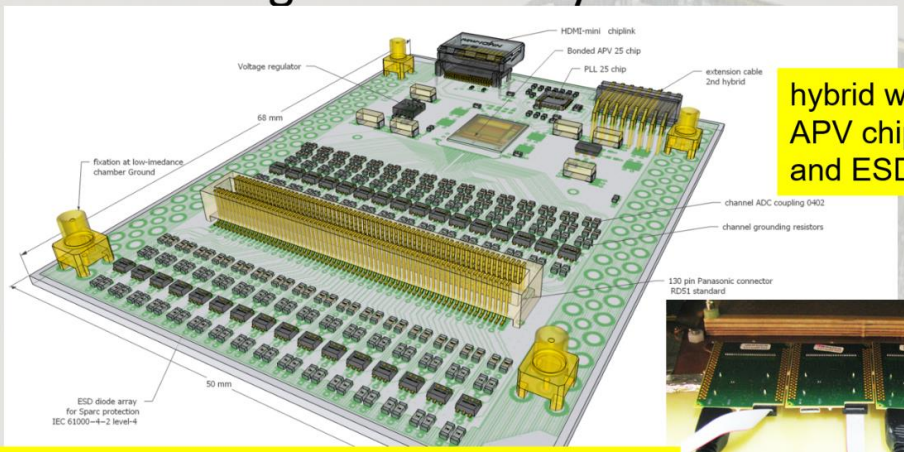


* Long HDMI cables up 30m possible with
Pre-De-emphasis equalization of LVDS on both ends

SRS scalable readout system

Initiative 2009: Development of portable multichannel data acquisition systems for RD51 detector studies

SRS “plug&play”
-keep the backbone system
-exchange the ASIC hybrid on the detector



hybrid with 128 channel APV chip and HDMI readout and ESD sparc protection

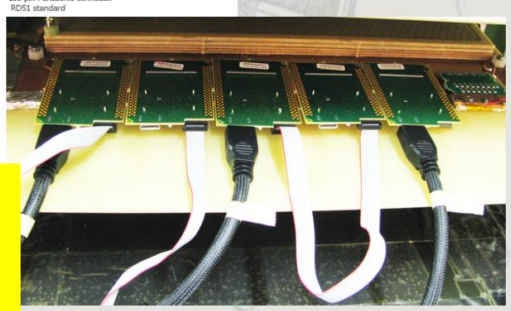
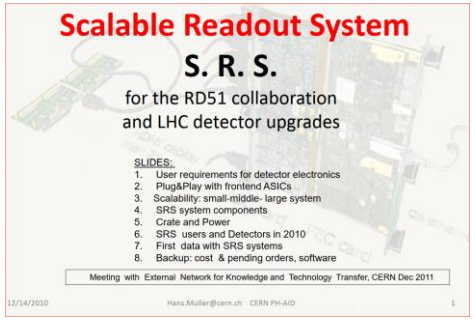


photo of APV hybrids on GEM chamber readout via HDMI cables

All SRS hybrids have a standard detector- and readout- interface.

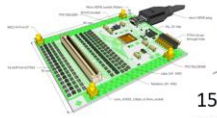
Individual hybrids have different readout ASICs



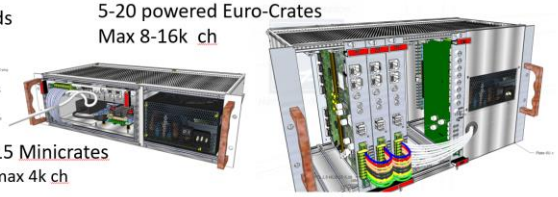
Presentation to
Industry Liaison Officers
CERN 2010

estimated SRS-classic need 2013

500-1500 APV hybrids

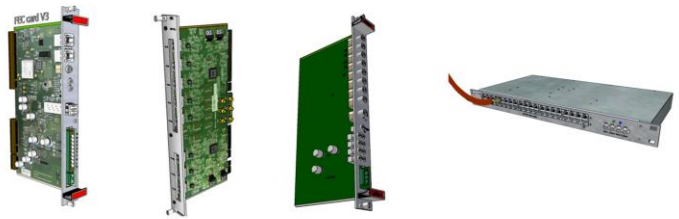


5-20 powered Euro-Crates
Max 8-16k ch

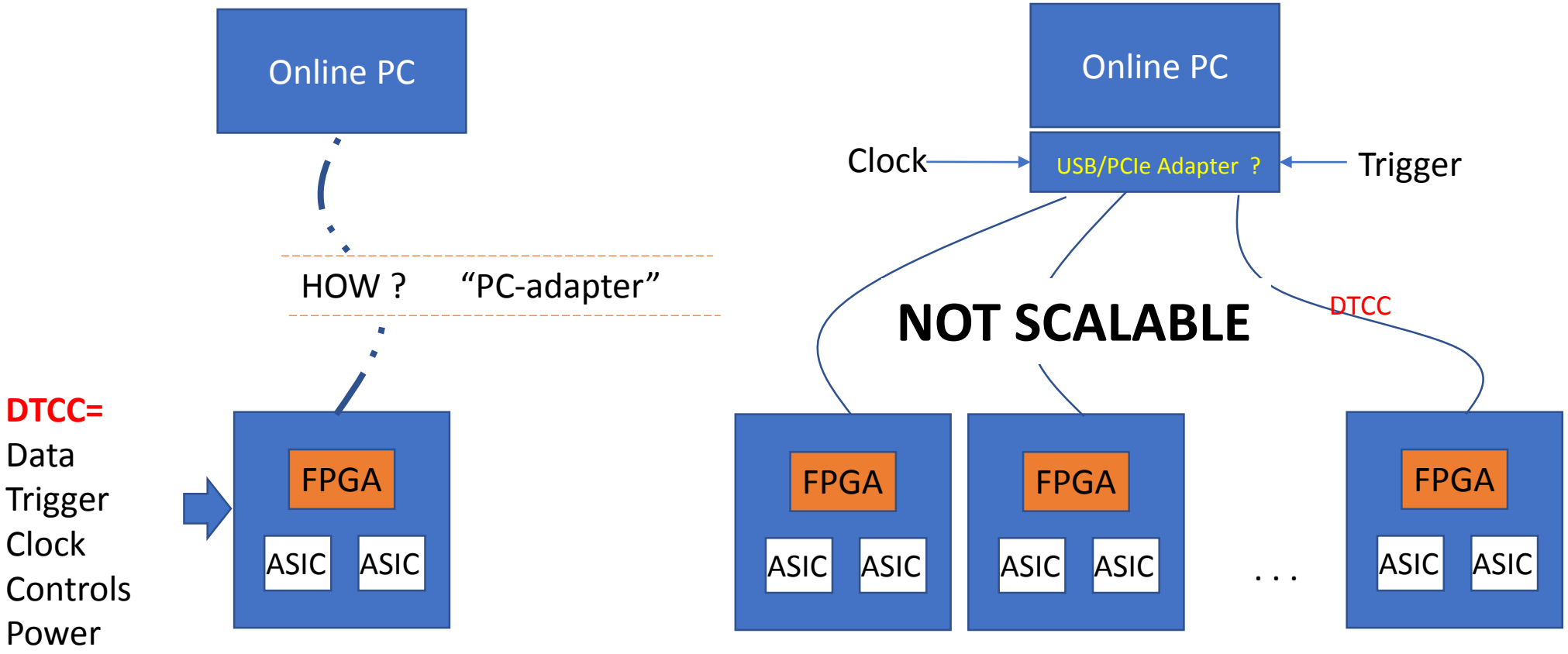


15 Minicrates
max 4k ch

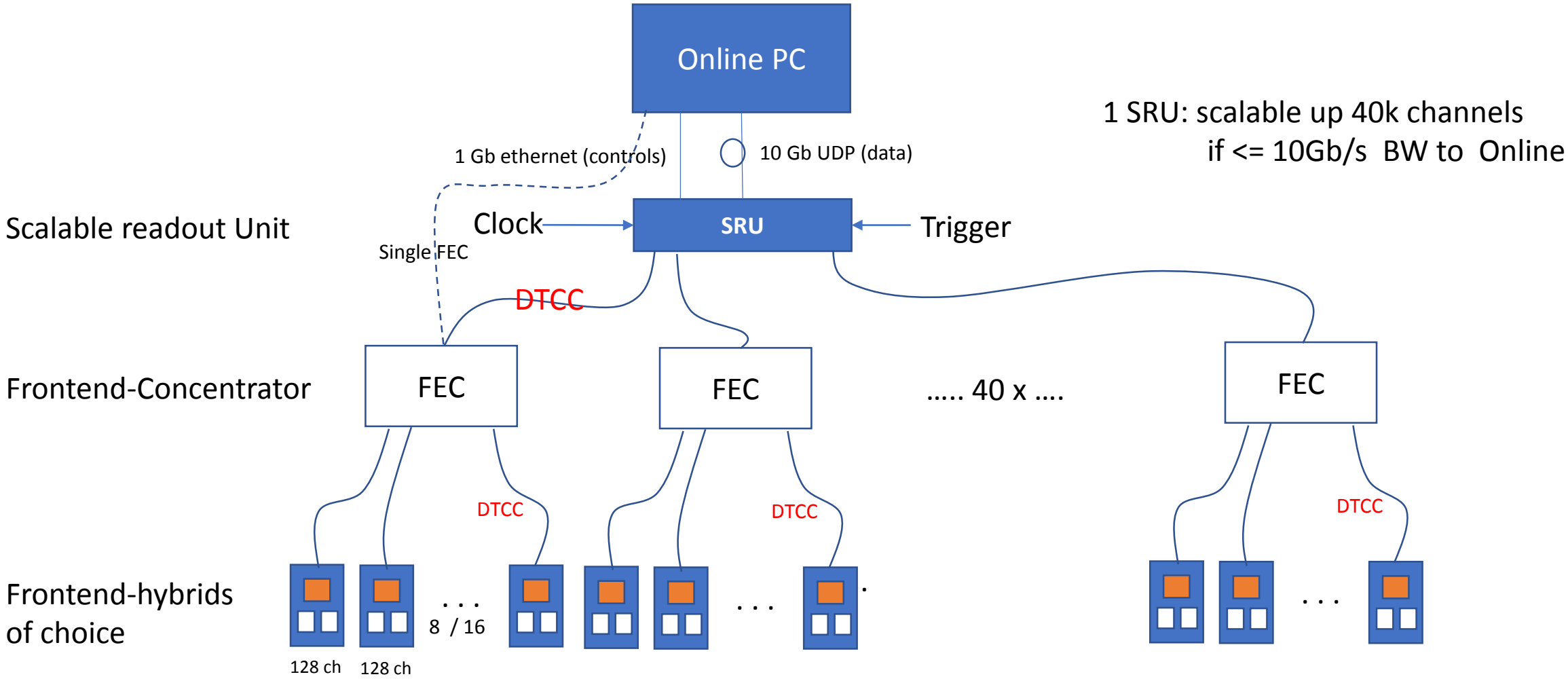
25-50 FEC cards 25-50 ADC cards 5-10 CTF cards 10-20 SRU boxes



Basic SRS idea: from ASICs to Online

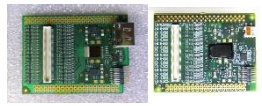
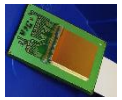


Scalable SRS concept (so far)



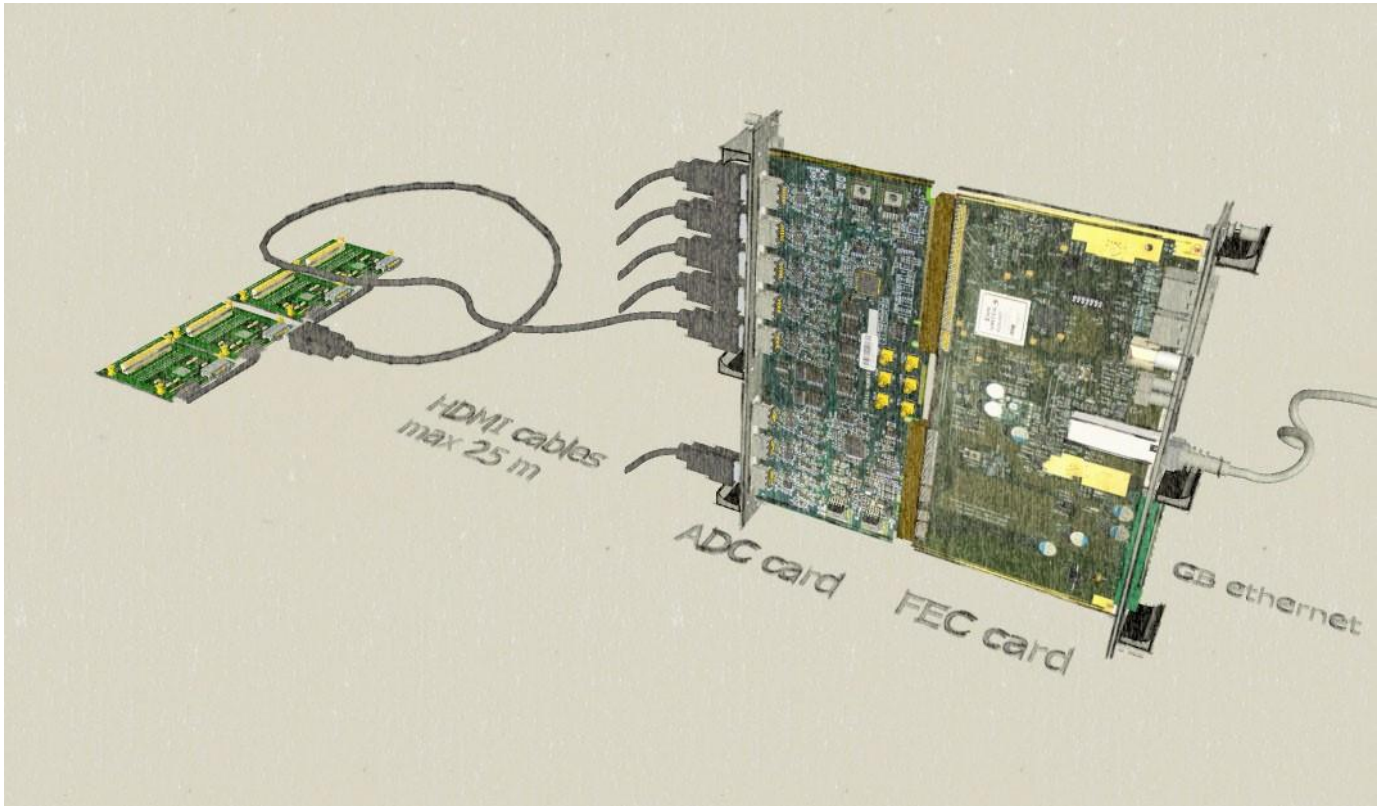
1 SRU: scalable up 40k channels
if <= 10Gb/s BW to Online

SRS frontends

APV25-RD51		V1,V2,V3 proto hybrids V4 became “working horse” up today
SiPM-NEXT		2 prototypes ATCA -SRS became standard for NEXT TPC
Timepix Univ.Bonn		2 prototypes A -> C-card -> AIDA project became Timepix 3 SRS
VFAT-RD51		V1 prototypes hybrid, discontinued, technical problems
Beetle RD51		V1 prototype hybrids, discontinued, bonding problems
GEMROC-AGH/EicSys		AIDA-project: GEMroc hybrid with plugin adapter for SRS
VMM-RD51		V1,V2,V3 proto hybrids, **V4 and V5 becoming new standard since 2018**

successful frontends: many man years and resources for HW, FW, SW*

“Workhorse” frontend for SRS since 2011
APV25 … less 1 Watt/hybrid readouit over HDMI

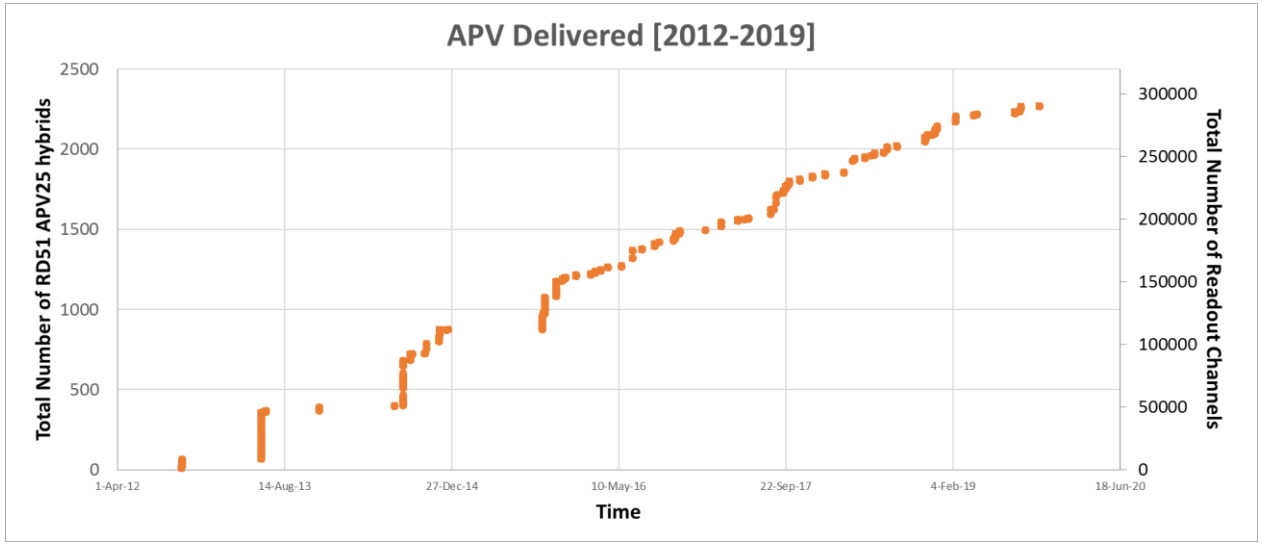


analogue APV circuitry is “tolerant” against power variations over cable, low voltage drop

SRS acceptance by RD51 teams

SRS phase 1 (APV frontend)

- R&D: laboratory and RD51 test beam: trackers (GEM and MM) and several MPGD under test (GEM, mm, THGEM, μPIC, RPWELL, μRWELL,..)
- LHC Upgrades: ATLAS R&D for NSW MM, CMS GEM QA&QC
- Experiments: TOTEM@LHC (FEC), NEXT@LSC(FEC), PRAD@JLAB

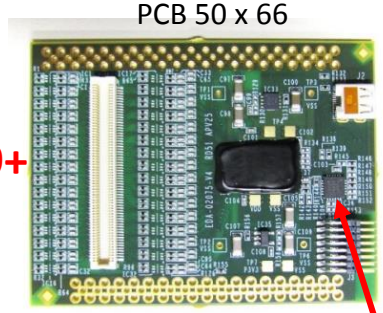


By 2014 O(100) deployed **SRS** test systems

~ 2500 APV SRS hybrids (**320k readout channels**) produced and sold in period 2012-2019 via **CERN store**

SRS frontend from APV25 to VMM3a

PCB 50 x 66



APV 2011-2019+

Pansonic connector

PLL chip

- **Analogue**
- 128 channels with single chip
- AC coupled 100pF
- Master or Slave
- Embargo list countries
- 1/2 W per hybrid
- Cooling negligible
- No zero suppression
- Ext. level-0 trigger required
- Max trigger rate **O(5kHz / hybrid**)
- timing resolution O(~5 ns)
- No clustering logic
- fixed preamp gain 65mV/fC polarity selectable
- fixed peaking time 50 ns in peak mode
- Noise ca 2000 e- @ C_{det}~ 50 pF
  (246 e + 36e-/pF in peak mode)
- max. detector Capacity C_{det} ~ 50 pF
- fixed CSA gain -> dyn. range 50 fC
- linear up 4 MIPs

PCB 50 x 85

VMM 2019 +

HRS connector

FPGA, Flash and uADCs

- **Digital**
- 128 channels with 2 VMM chips
- AC coupled 470 pF @ 1M with TVS spark protection
- Master = Slave
- No embargo, but BNL licence may apply to non-RD51 teams
- 3.5W per hybrid, 2 supply voltages P2~ 1.8V(3W),P1 ~3V(0.5W)
- Cooling important (convection cooler = standard, water pipes optional)
- Self-triggered with Zero suppression
- Continuous or level-0 triggered mode
- ART flag + 7 bit 1st hit address withing BCID period
- Trigger rates **O(4 MHz /channel)**
- timing resolution O(1ns) 8bit TDC
- Neighbor detection below threshold for higher space resolution
- 8 different preamp gains 0.5-16mV/fC , polarity selectable
- 4 different peaking times 25- 200ns
- Charge resolution 10 bit ADC (7bit in current 3a version)
- channel pulser programmable via 10 bit DAC up 1V
- analogue monitoring: selected channel sheper peak and time
  temperature, baselines etc, SRS hybrid readout via 12bit uADC , I2C
- Noise 500e- intrinsic, 1300 e- @ C_{det} ~ 50pF
- max. detector capacity C_{det}~ 2nF in high capacity mode
- CSA linear dynamic range up 2 pC @ gain 0.5mV/fC

Hans.Muller@cern.ch

SRS frontend hybrid (VMM)

ASIC VMM3a

130 nm Global Foundries 8RF-DM-8LM process
die size 15.308 × 8.464 mm2
multiproject 200mm wafer 113 VMM dies per wafer
unlkike ATLAS: wafers are not thinned, dies not packaged

Wire bonding

Commercial Alu wire bonding: 2 x VMM dies
426 pads per die

Hybrid size and weight

80 x 50 mm, 140 pin HRS connector, 128 VM channels, 100g cooler incl.

Spark protection

external ! TVS diodes and 1M resistor from each detector ch. to GND
470 pF ac coupling to channel input

Power

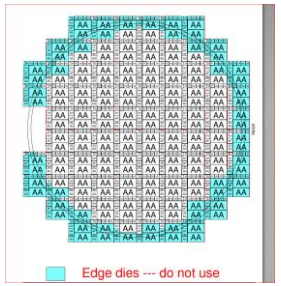
analog and digital 1.2V ca. 1 Watt per VMM3a die
External Power to 5 x onboard LDOs 3W
P2 =1.8V @ 1.7A (2 x VMM)
P1 = 3V @ 0.2A (FPGA, Flash, uADCs etc)
3 pin snap-in connector for power cable

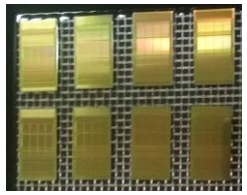
Cooling

custom produced convection cooler with
bottom side deflection plate. Option for 4mm dia cooling pipes

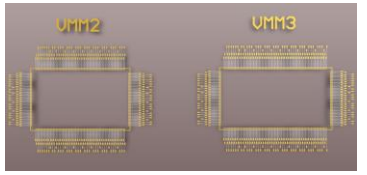
Temperature

die temperature max 60C with convection cooler typ. 50C





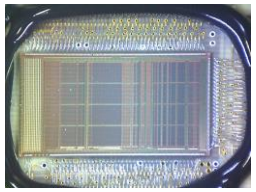
Laser-diced VMM chips

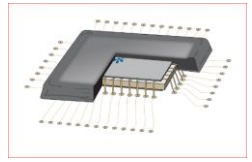


Wire bonding pattern

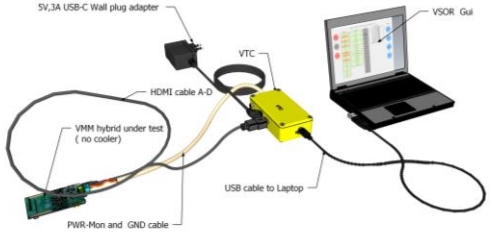
200 mm multiproject wafer : 113 good dies

Wire bonding on high-tech PCM

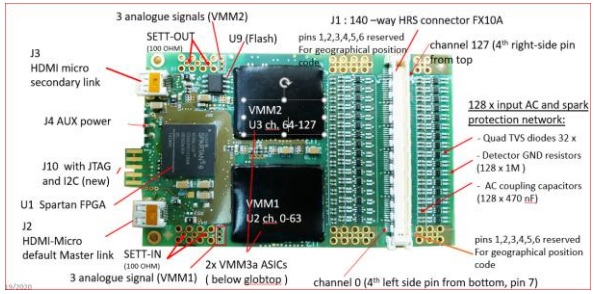




Globtobbing (shown: dam around chip)



VTC test power and baseline
Results + serial No -> database
bad chips get re-bonded



VMM3a hybrid connectivity

Custom Convection cooler with water pipe option

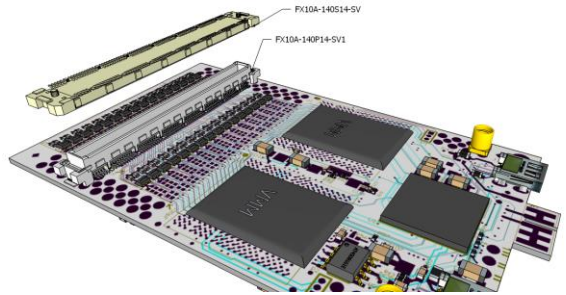
Connectors: Frontend <=> MPGD detectors

Note: previous Panasonic connectors are obsolete, you may need adapters

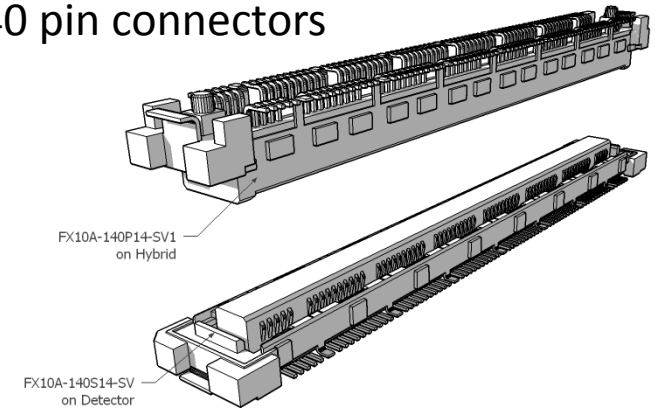
Strip pitch:

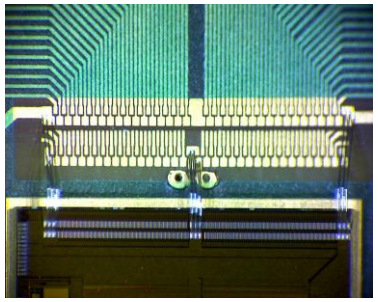
readout strips / pads : O(128)ch/50 mm -> **400um default**

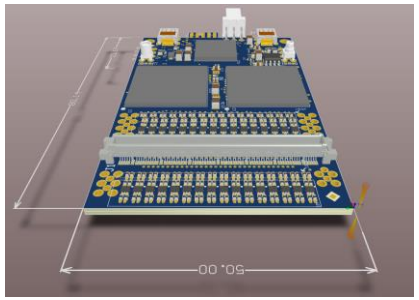
-> 128 ch-connector fixed on MPGDs (**HRS 140 pin standard)**

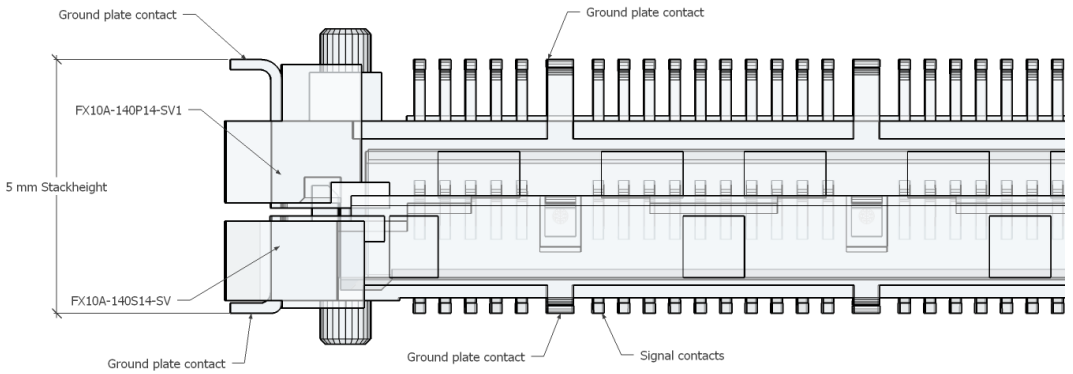


HRS 140 pin connectors







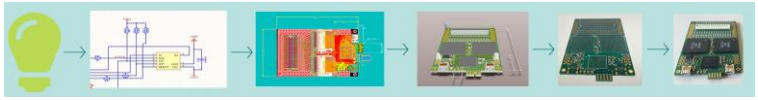


14 GND pins for low impedance GND to detector
2 groups of 6 spare pins for
a.) geographic position code b.) I2C bus to detector resident sensors

2019+ SRS procurement & production

See also:talk of Eraldo Oliveri in WP 3.35 AIDA-innova 13.04.2021

- VMM hybrids and DVMM



Large involvement in design, pilot production and debugging from SRS Technology (spinoff with CERN KT lisence)

First “large” VMM hybrid production 2020

So far ~500 hybrids produced and deployed
~ 10 teams/experiments
2021/22: 1700 more in pipeline

First large production totally outside CERN

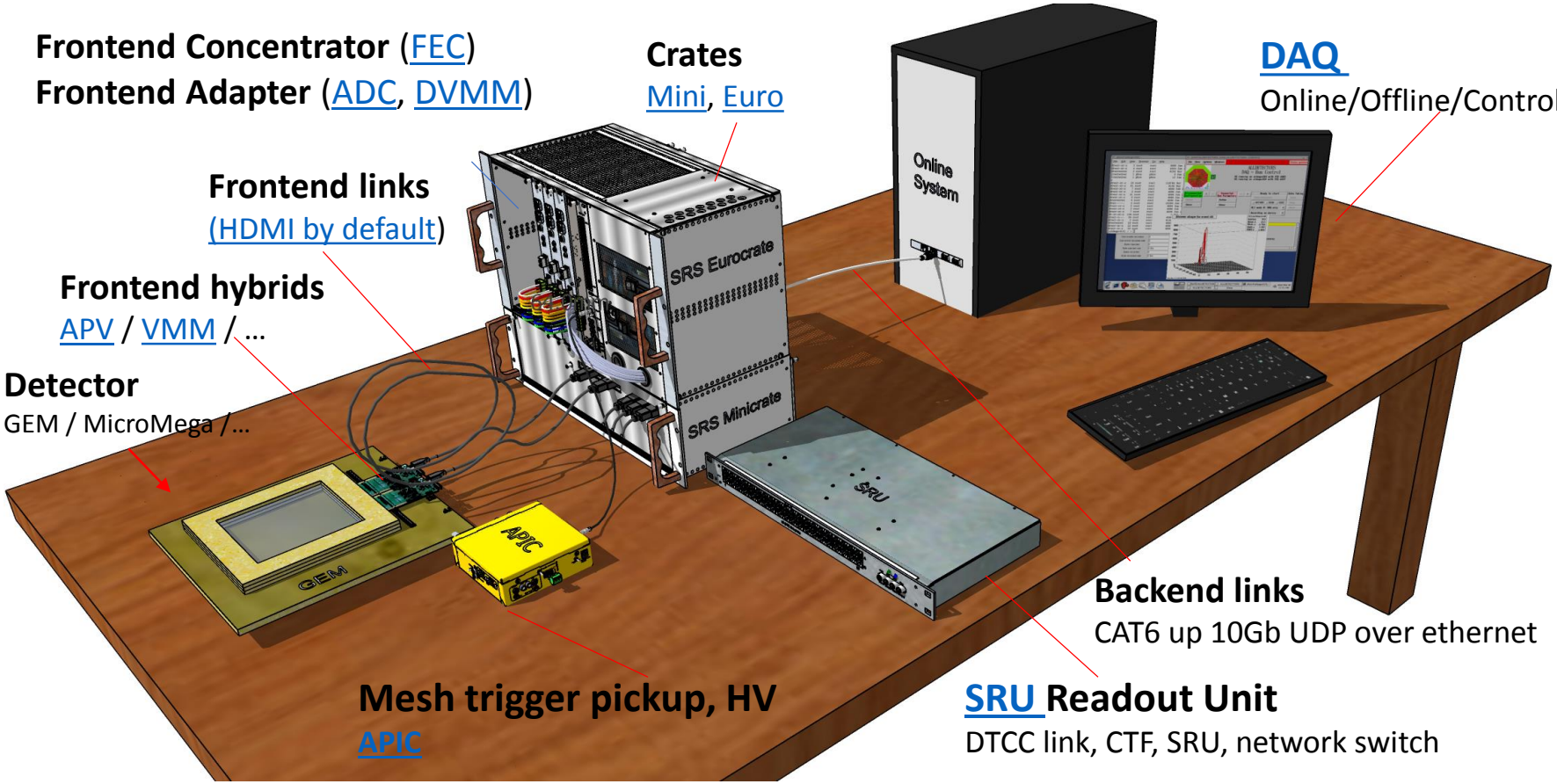
- FEC card

distribution via CERN store
O(200) in use
option of direct purchase from producer Samway Electronics

Passive cooling and DVMM card

SRS system components

table-top test systems



DAQ, slow controls and analysis for SRS-VMM

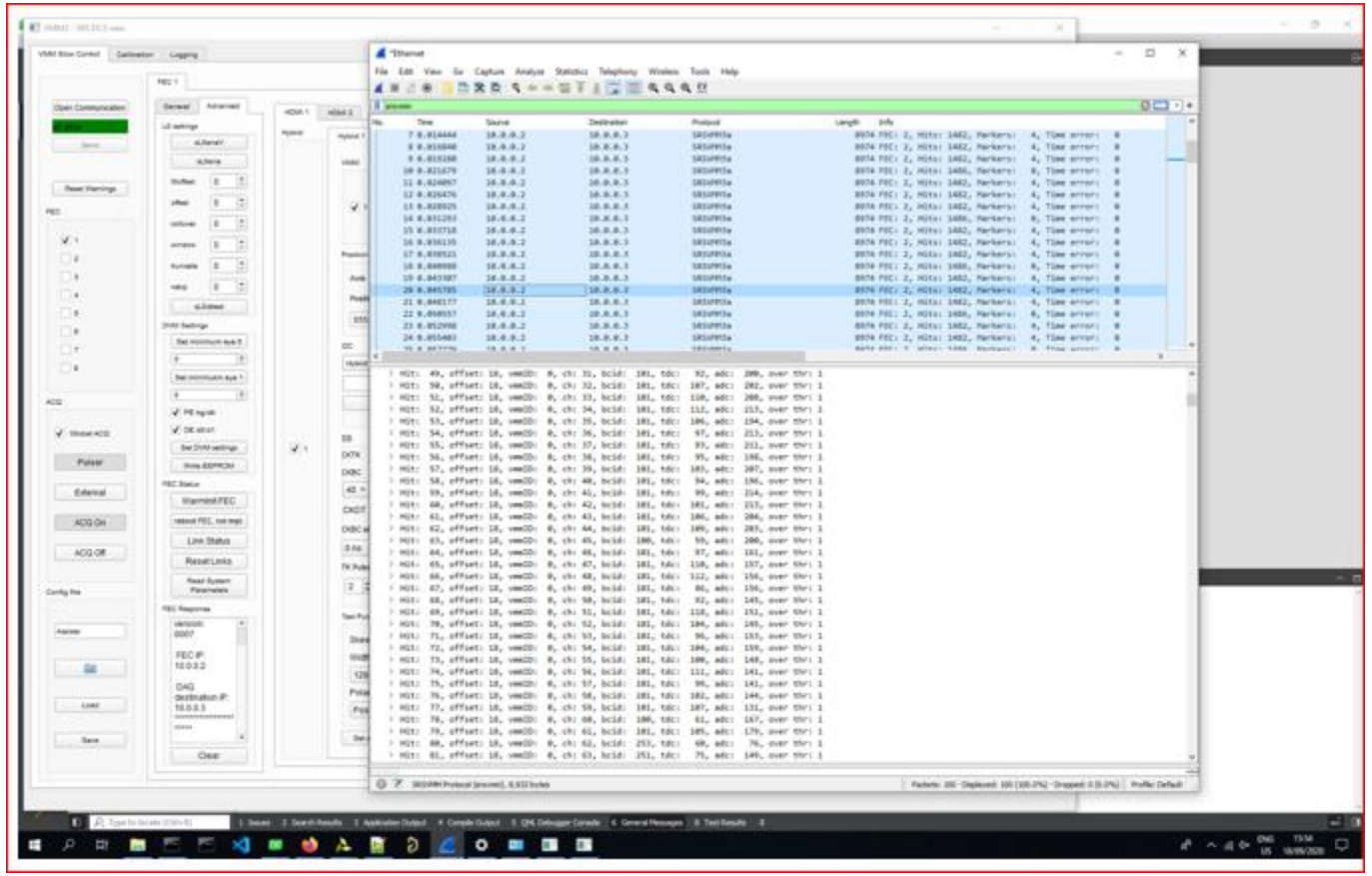
ESS DAQ : stable ad mature DAQ system with slow controls and
vmm-sdat analysis (data fitting with alglib)

Runs on Ubuntu 18 on a PC with min.
16 GB RAM, 2 network cards 10Gb and
Jumbo frame support

Install also wireshark and Xilinx Impact

Designed to become standard for ESS
and is (free) available to all SRS VMM users

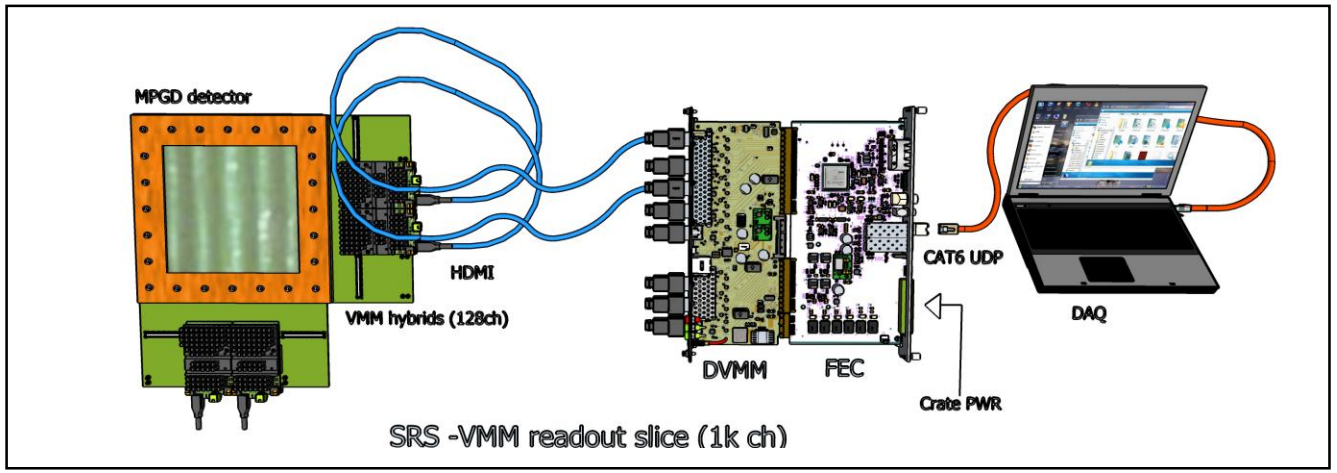
See talk Dorothea Pfeiffer in WG5 15 Feb 21



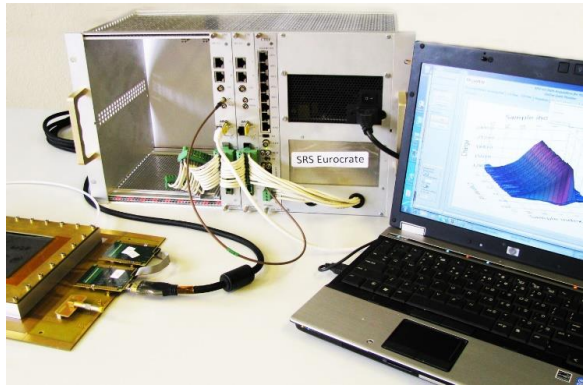
DAQ repo https://gitlab.cern.ch/rd51-slow-control/vmmsc/-/tree/ESS
Slow controls repo: https://gitlab.cern.ch/rd51-slow-control/vmmsc

Starter systems

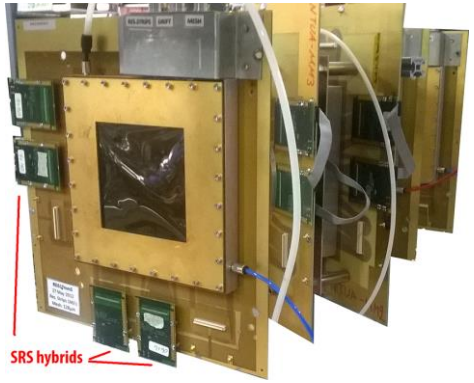
1-8 hybrids (128 – 1k channels) requiring 1 FEC + 1 DVMM + 1 Minicrate



Laboratory detector tests with radioactive sources



Testbeams



SRS Crates (19 inch standard)

Eurocrate 8k Slots:

8k channels
8 FEC cards + 2 DVMM cards
1 CTF card (common clock and trigger)
64 HDMI ports (rear side)

Eurocrate Power:

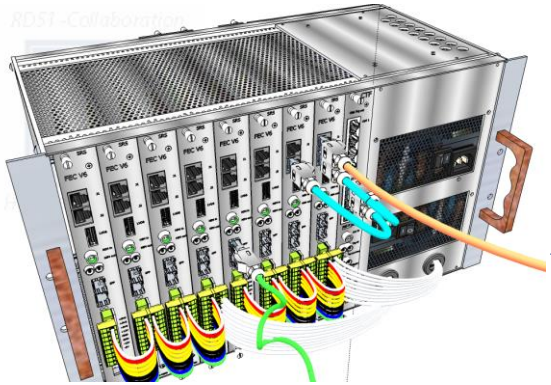
2x500 Watt ATX with SRS power converter/filter
Power bus for 8 FEC and 1 CTF
Power for up to 64 VMM hybrids via DVMM

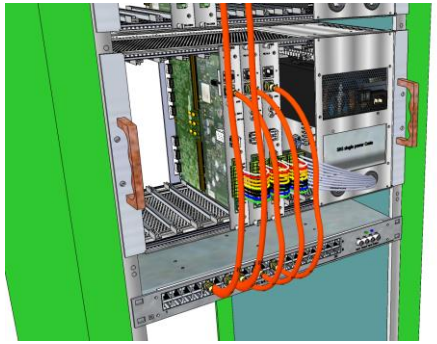
Minicrate 2k Slots:

2k channels
2 FEC cards + 2 DVMM cards
1 CTF card (common clock and trigger)
16 HDMI ports (rear side)

Minicrate Power:

450 Watt ATX with SRS power converter/filter
Power bus for 2 FEC and 1 CTF
Power for up to 16 VMM hybrids via DVMM





Rack in counting room

Custom-built 19’ Crate mechanics (ATOS)
SRS power converter: SRS technology

FEC cards: Frontend Concentrator

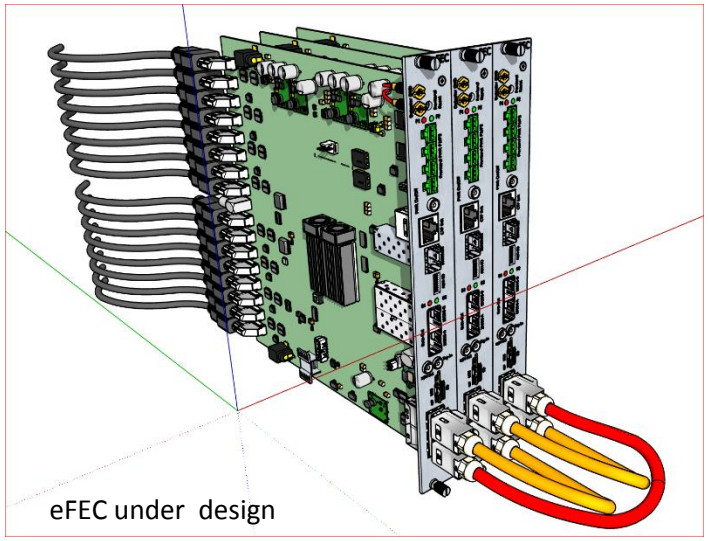
FEC V6 (standard since 2013)

- Virtex 6 FPGA with network support (UDP)
- 2 x SFP+ ports, 3 Gbit each
- NIM I/O and 2x RJ45 for DTCC links
- 3 x PCIe connectors for SRS adapters (DVMM)
- plugin-DDR3 memory 2 Gbyte

eFEC (2021 , ongoing collaborative effort 2021)

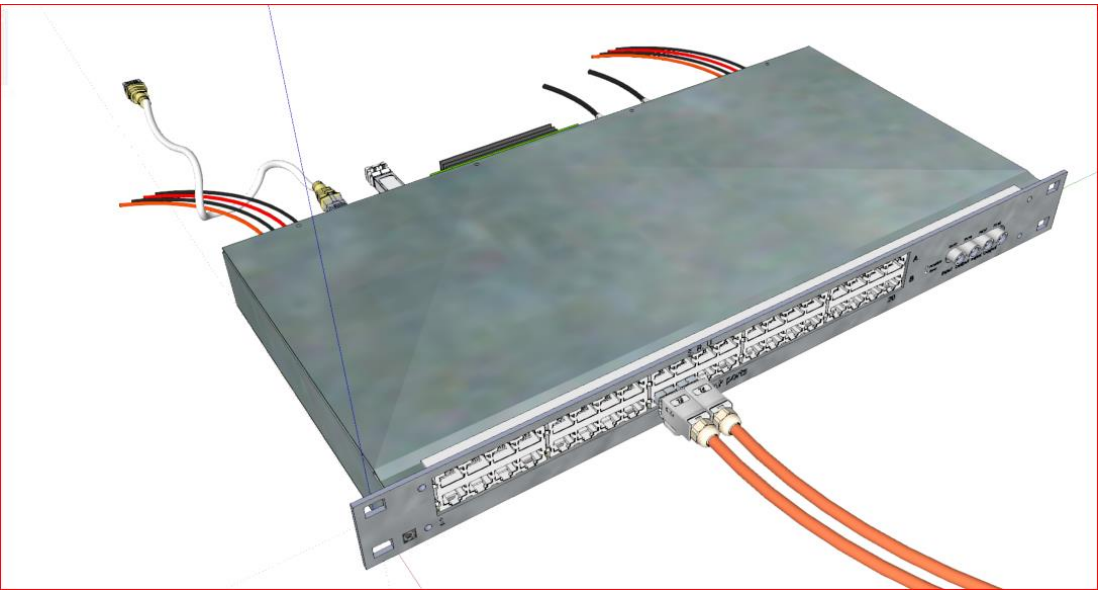
- Ultrascale+ Zynq (SoC) FPGA
- 2 x SFP+ ports, 10 Gbit each
- universal link adapter included (replacing DVMM)
- plugin-DDR4 memory 16 Gbyte
- power / housing in same SRS crates as FEC
- X-bus: horizontal message passing (triggers)
- Synch-bus (common signals, Busy , Reset etc)
- CTF link: common clock/trigger distribution

FEC V6 cards



eFEC under design

SRU Scalable Readout Unit



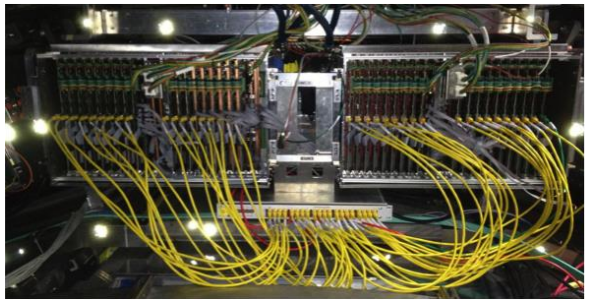
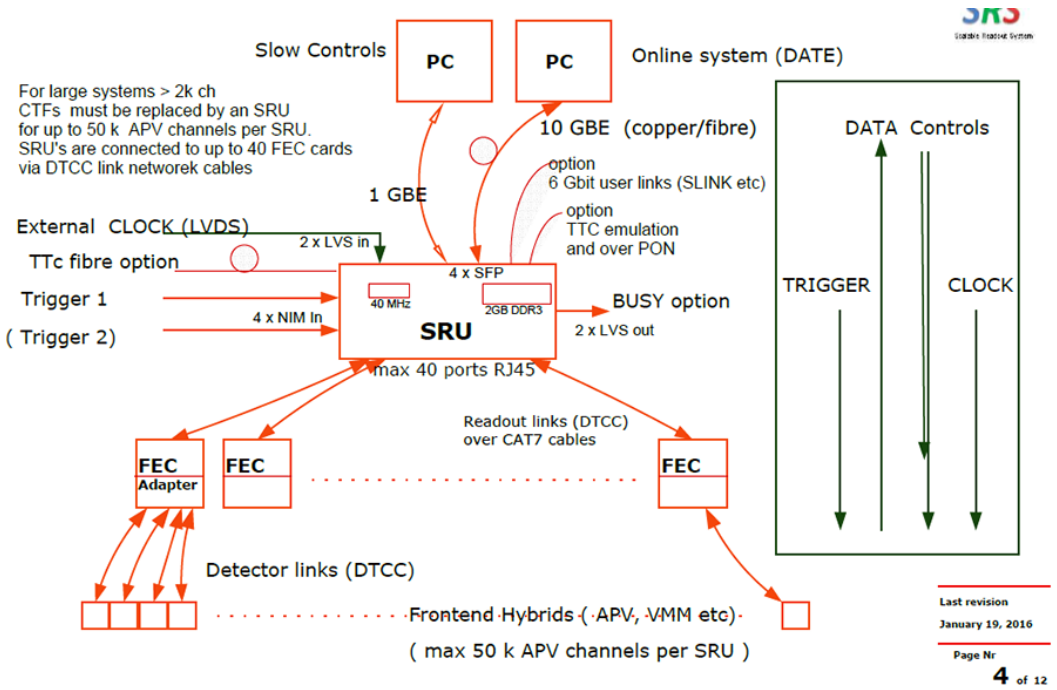
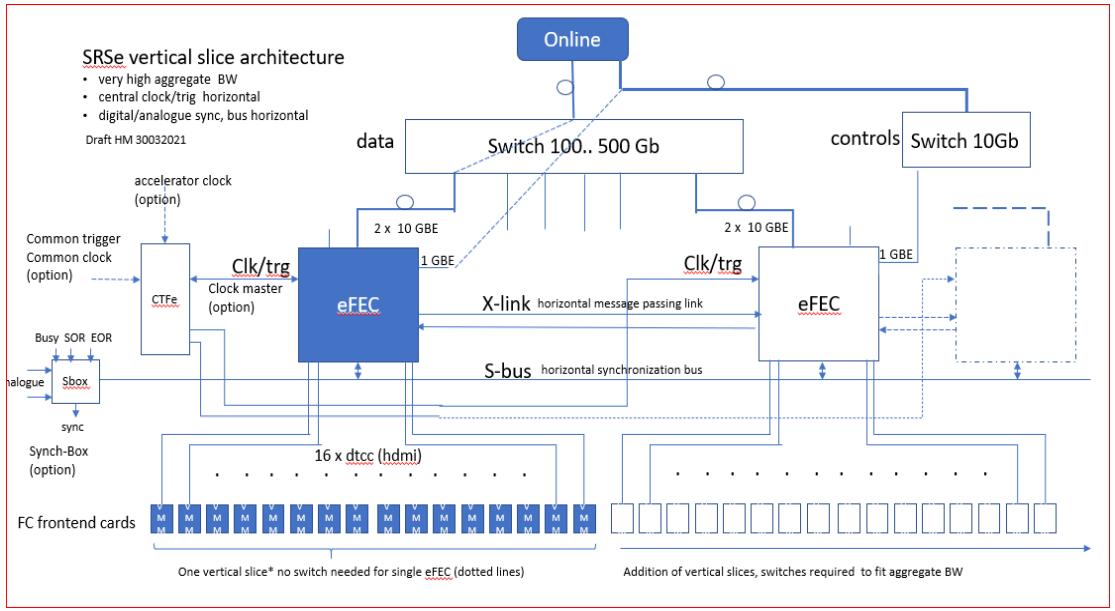
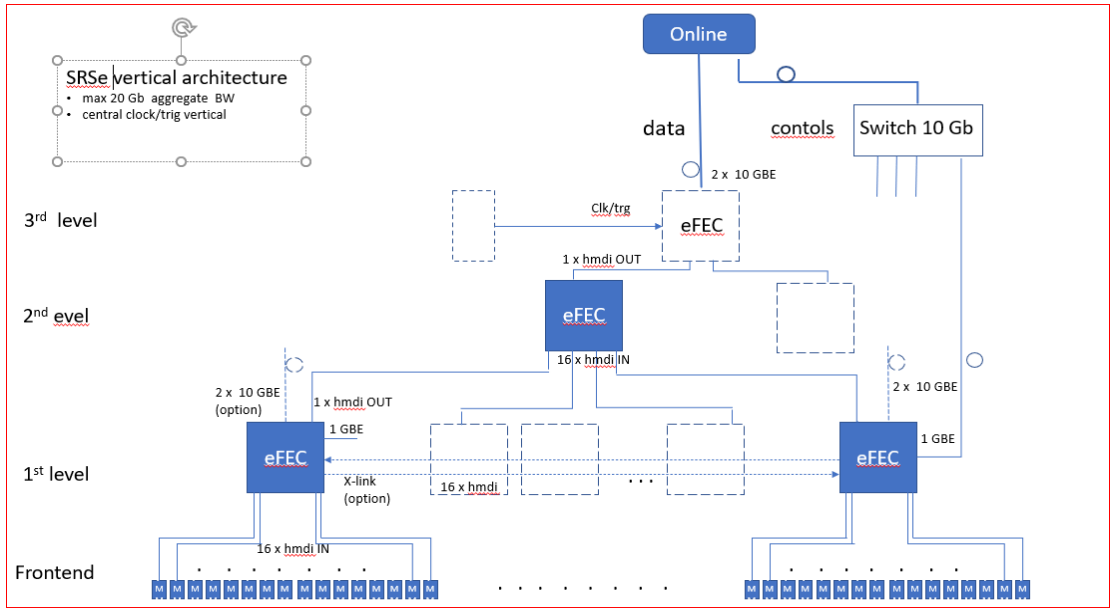


Photo: SRU with 40 DTC links in one ALICE EMCaL sector



New SRSe* architectures (eFEC-based)





Flat: addition of vertical readout slices

central clock distributed via CTF
horizontal trigger & syc. buses
BW limited by data switch (500 Gb/s)
event-building in Online farm

Hierarchical :

central clock from top level eFEC
event-building in top level eFEC
BW limited by top-level eEFC (20 Gb/s)

* Snowmass LoI IF7-IF5 (replace PBX by SRSe)

New frontends for eFEC

under discussion

SAMPA (see presentations Marco Bregant in WG5 miniweeks)

designed for ALICE TPC upgrade
digital shaper with baseline correction
SRS-like hybrid under design in Sao Paolo
eFEC interface under discussion

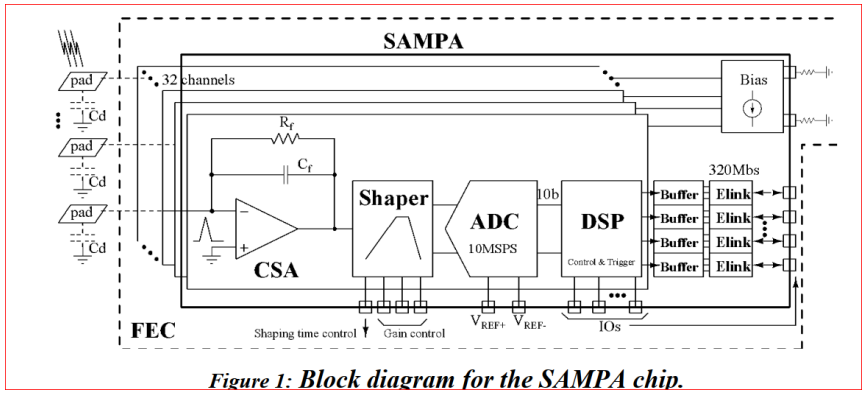
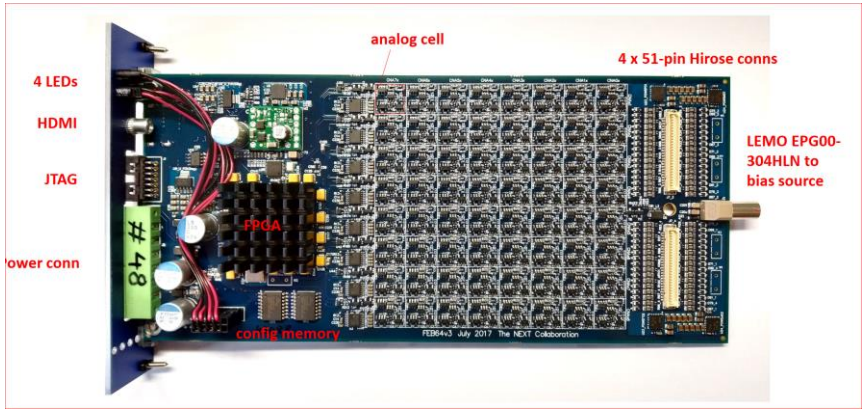


Figure 1: Block diagram for the SAMPA chip.

SiPM frontend chip for NEXT

planned
NEXT readout based on **ATCA variant of SRS**
Upgrade to fit with eFEC universal link adapter
hierarchical architecture with DDR4 buffer



Collaboration on SRS with ESS

Neutron scattering facilities near Lund

Decision to use "RD51 hybrid" for readout of Gd-GEM detector

Joint SRS –VMM readout project @CERN GDD lab:

firmware and software collaboration
NMX detector with VMM based SRS readout

NMX detector:

1 m2 GEM with 250um Gadolinium n-converter sheet
use uTPC concept of ATLAS NSW

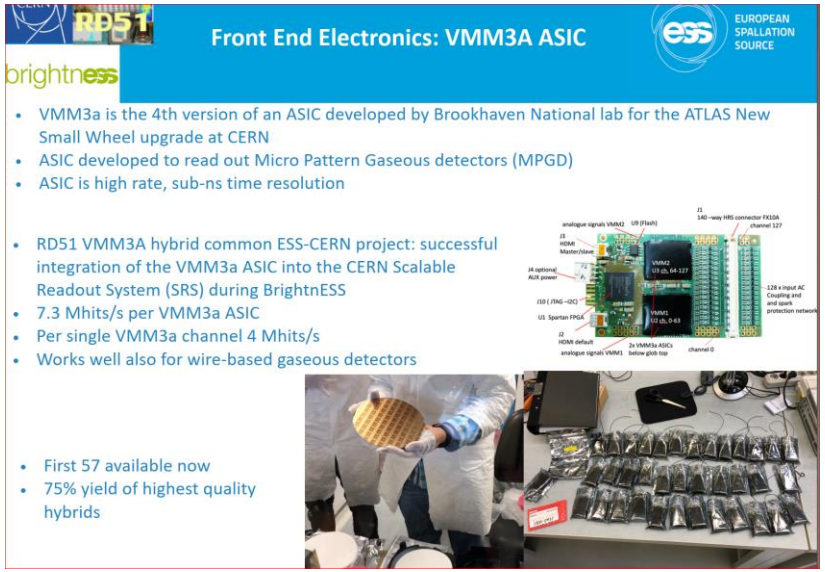
ESS contributions to SRS (see talks Dorothea Pfeifer in WG5 meetings)

DAQ software and slow controls for SRS-VMM

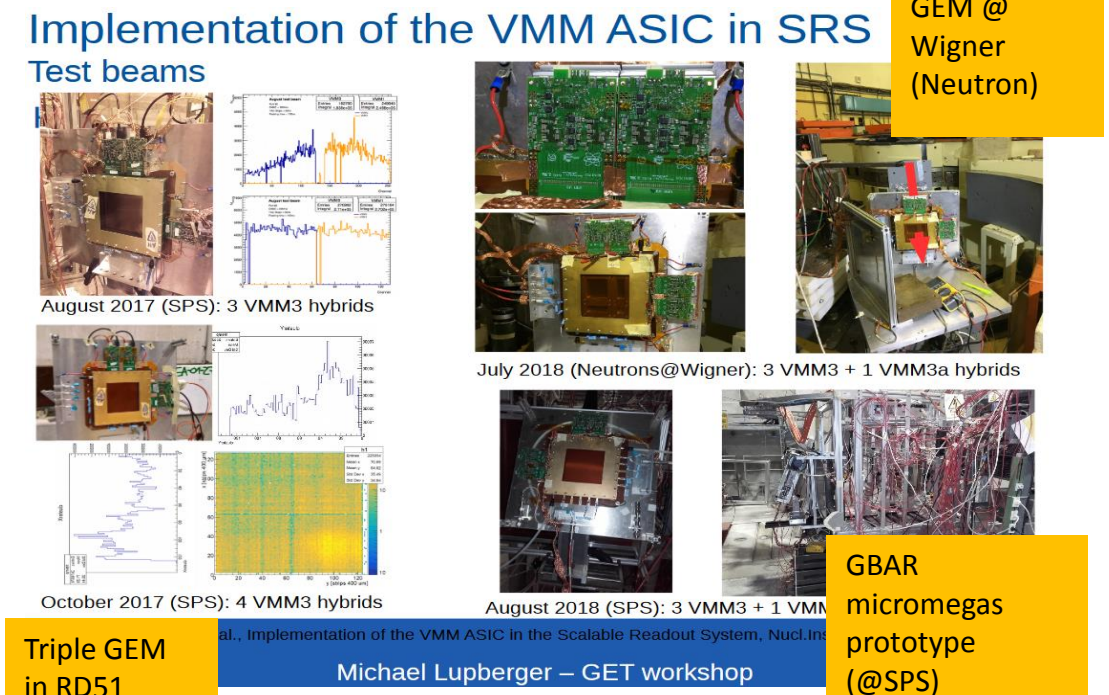
Joint projects (incl. several project students)

readout commissioning full system on NMX detector
firmware revision FEC FW
addition of DDR3 readout
VTC test firmware and documentation VMM hybrids
eFEC option with Ultrascale+ technology

See talk R. Hall-Wilton CERN Detector Seminar 4 Dec. 2020



Pilot systems (testbeams)



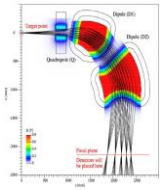
ESS Triple GEM @ Wigner (Neutron)

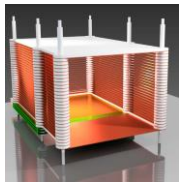
Triple GEM in RD51 Tracker @ SPS

GBAR micromegas prototype (@SPS)

https://indico.in2p3.fr/event/17431/contributions/66506/attachments/50812/65014/GET_Workshop_Bordeaux_MLupberger_SRS.pdf

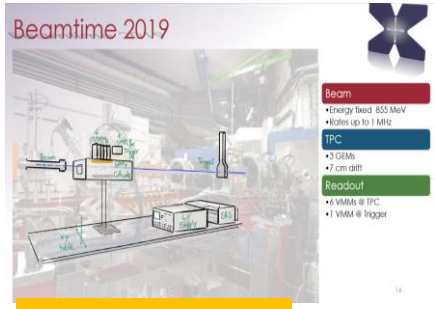
See talk of Eraldo Oliveri in WP 3.35 AIDA-innova 13.04.2021



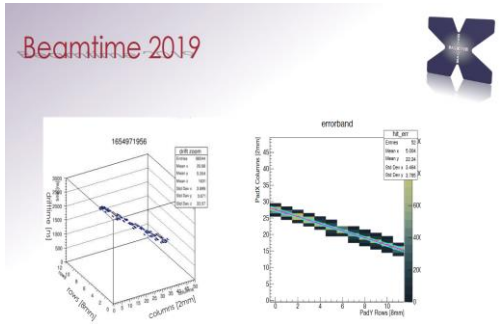


MXTPC (Pepe Gulker, RD51 mini week, Feb 2020)

https://indico.cern.ch/event/872501/contributions/3743007/attachments/1985085/3307389/2002_rd51_miniweek_guelker.pdf



TPC Testbeam @ Mainz



Credits

technical contributors to the SRS readout system, related electronics , firmware and software, 2009-2021

Jose Francisco Toledo Alarcon, Jochen Kaminski, Joerg Wotschack, Paolo Iengo, Fan Zhang, Raúl Esteve Bosch, Givi Sekhniaidze, George Glonti, Pierre Salin, Eraldo Oliveri, Sorin Martoiu, Manuel Sanchez Suarez, Raffaele Giordano, Volkan Gezer, Kondo Ganvo, Markus Hohlmann, Filippo Costa, Marcin Byszewski, Manik Aima, Alfonso Tarazona Martínez, Andre Zibell, Alexandru Rusu, Michael Lupberger, Brian Doney, Michele Quinto, Adrian Fiergolski, Dorothea Pfeiffer, Vasilios Dimitris Karaventzas, Stefano Colafranceschi, Cosmin Jalba, Ignacio Lazaro, Byungchul Kim, Ryan Griffiths, Freddy Fuentes Robayo, Lucian Scharenberg, Jerome Samarati, Yan Huang, Marek Hradcek, Finn Jaeckel, Sorina Popescu, Francisco Garcia Fuentes, Patrick Schwaebig, and Hans Muller

+ many SRS users

The SRS project was/is motivated and financed by the RD51 collaboration with strong support by Leszek Ropelewski and Maxim Titov and at CERN by the managements of the CERN PH –DT and the ALICE PH-DAQ groups.

Major project resources were contributed by AIDA 2020 and by a standing collaboration with ESS Lund.

Licsencing, legal support and startup leverage was provided from the beginning of SRS via the CERN/KT department

Logistics of production and inhouse sales of SRS parts exists since 2010 via the CERN store

The following companies are/were included in prototyping and production: Prisma Electronics(GR), EicSys GmbH (DE), SAMWAY (RO), NEOHM (IT), ATOS(FR), SRS Technology (CH)