Future Requirements on Interconnection Technologies for Hybrid Detector Modules

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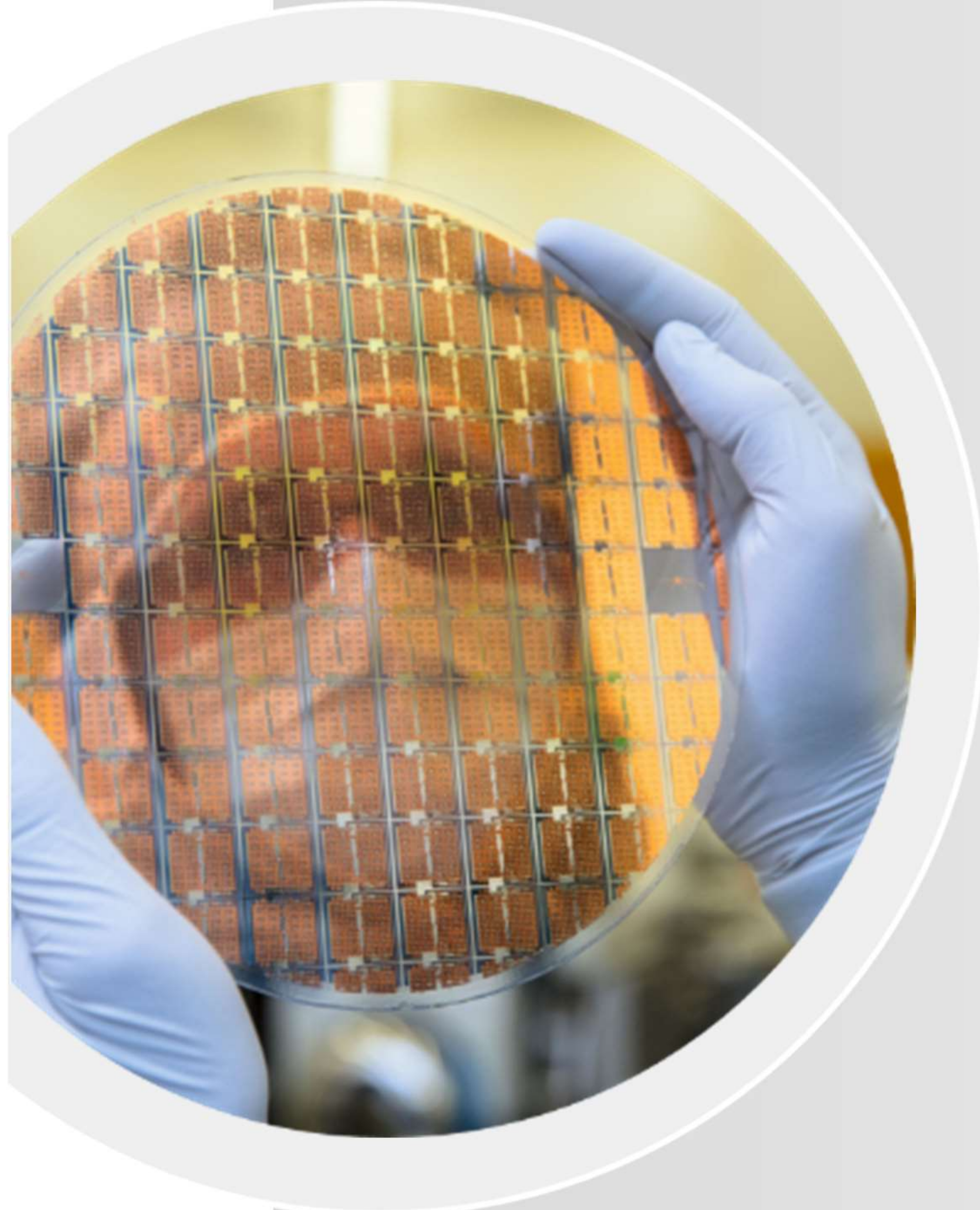
Fraunhofer IZM, Berlin, Dept. Wafer Level System Integration

ECFA Detector R&D Roadmap Symposium of Task Force 3 Solid State Detectors, March 23, 2021

Outline



- Wafer Level Post-Processing Technologies
  - Overview
  - Hybrid pixel module – status
- Flip Chip and Bonding Technologies
  - Flip chip technologies
  - Trends in interconnection technologies
- Advanced Integration Technologies
  - 3D TSV integration
  - Chiplet intergration
  - Embedding and Fan-Out packaging
  - Photonic packaging

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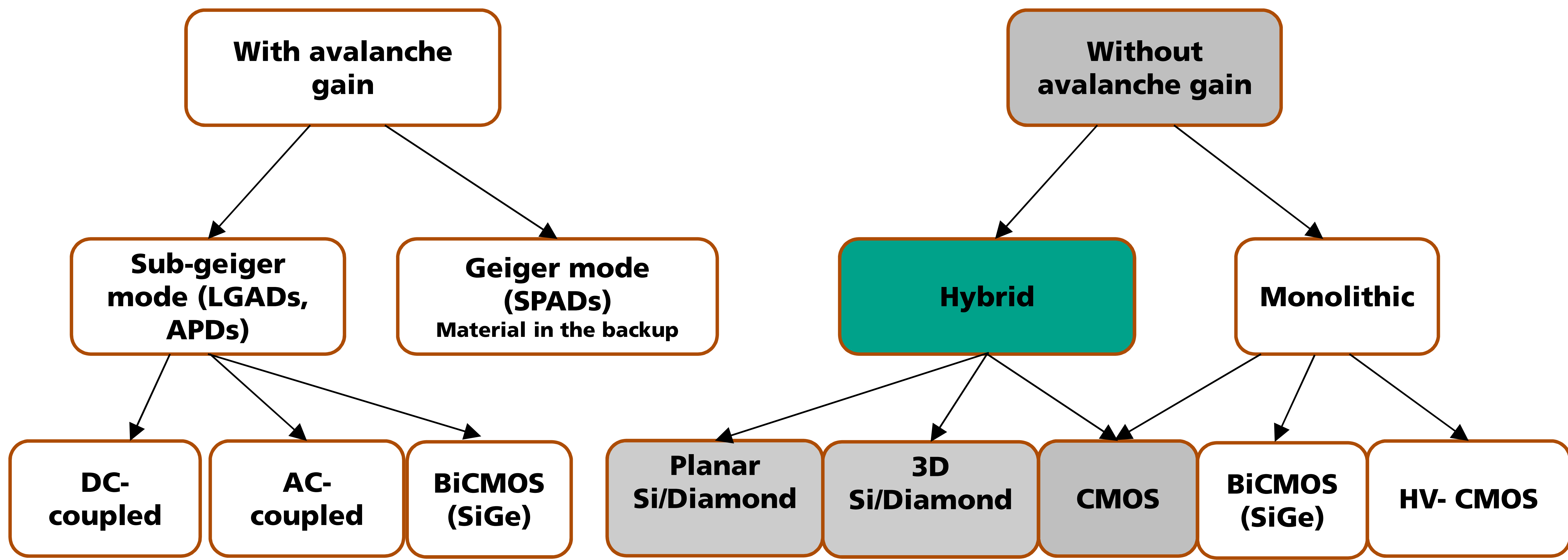
Solid state detectors for future (4D) trackers



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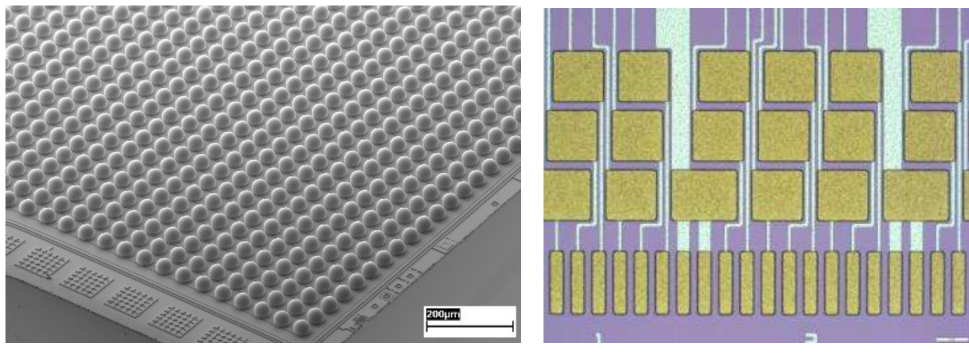
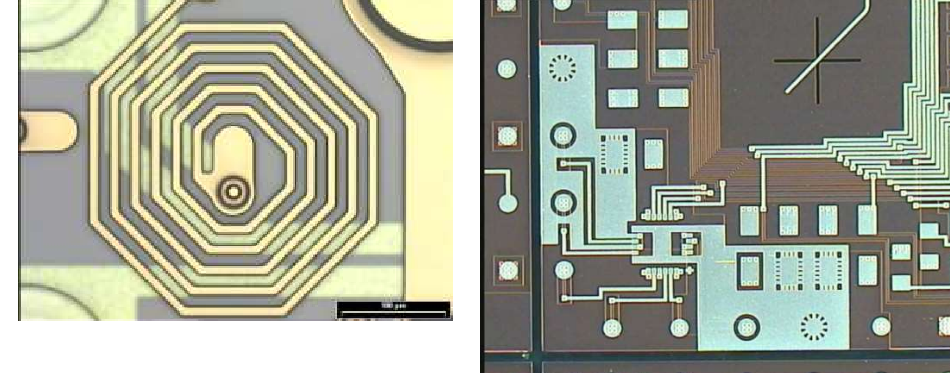
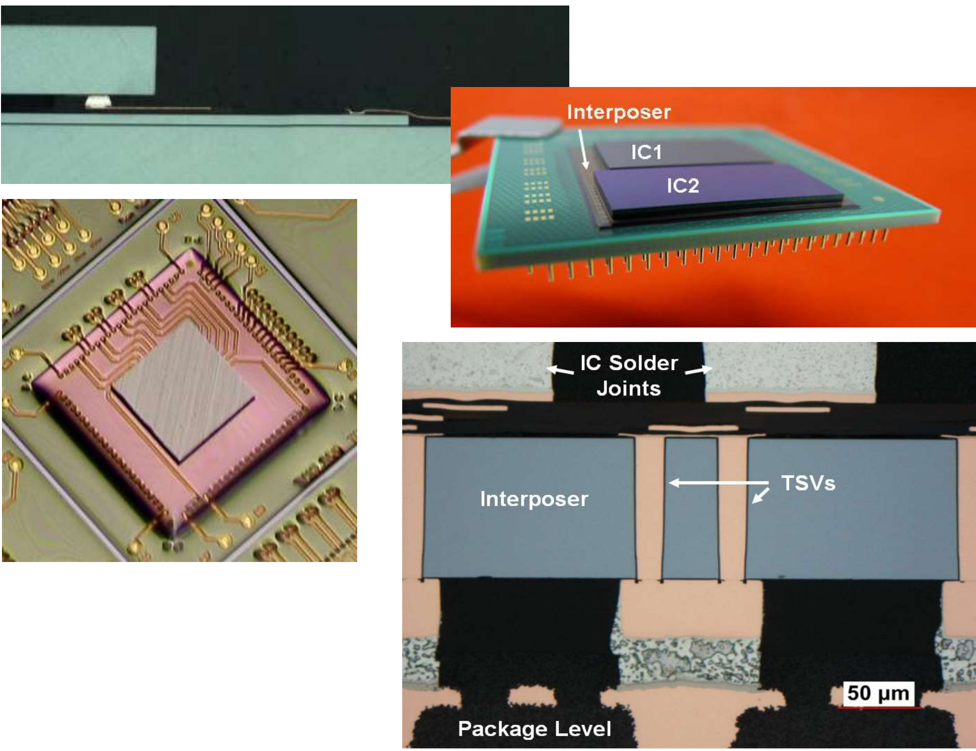
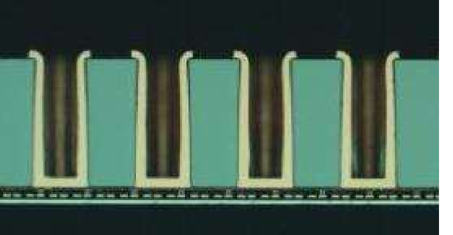
Wafer Level Post-Processing Technologies

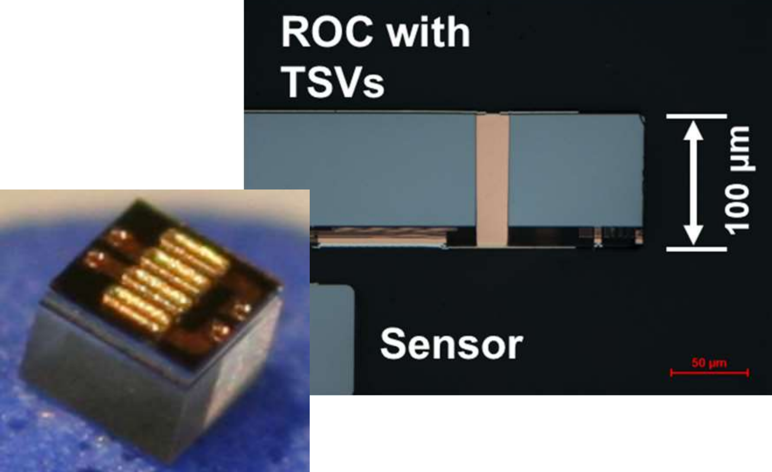
2D Wafer Level Packaging		2.5D System Integration		3D System Integration
Fine Pitch Bumping and Interconnects	Redistribution Layer with Integrated Passives	Chip on Chip Thin Chip Integration (TCI)	TSV Silicon Interposer	TSV in active IC











Complexity / Functionality / Integration

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Wafer Level Process – Example Wafer Bumping and Assembly

Seed Layer → Resist Process → Lithography → Plating → Strip / Etching → Dicing → Assembly

Sputter	Spin Coater	Mask Aligner	Wafer Plating	Wet Etching	Dicing	Flip Chip

Sputter Etching and Sputtering of the Plating Base / UBM

Spin Coating and Printing of Photoresist

Electroplating of UBM and Bump

Resist Stripping and wet Etching of the Plating Base

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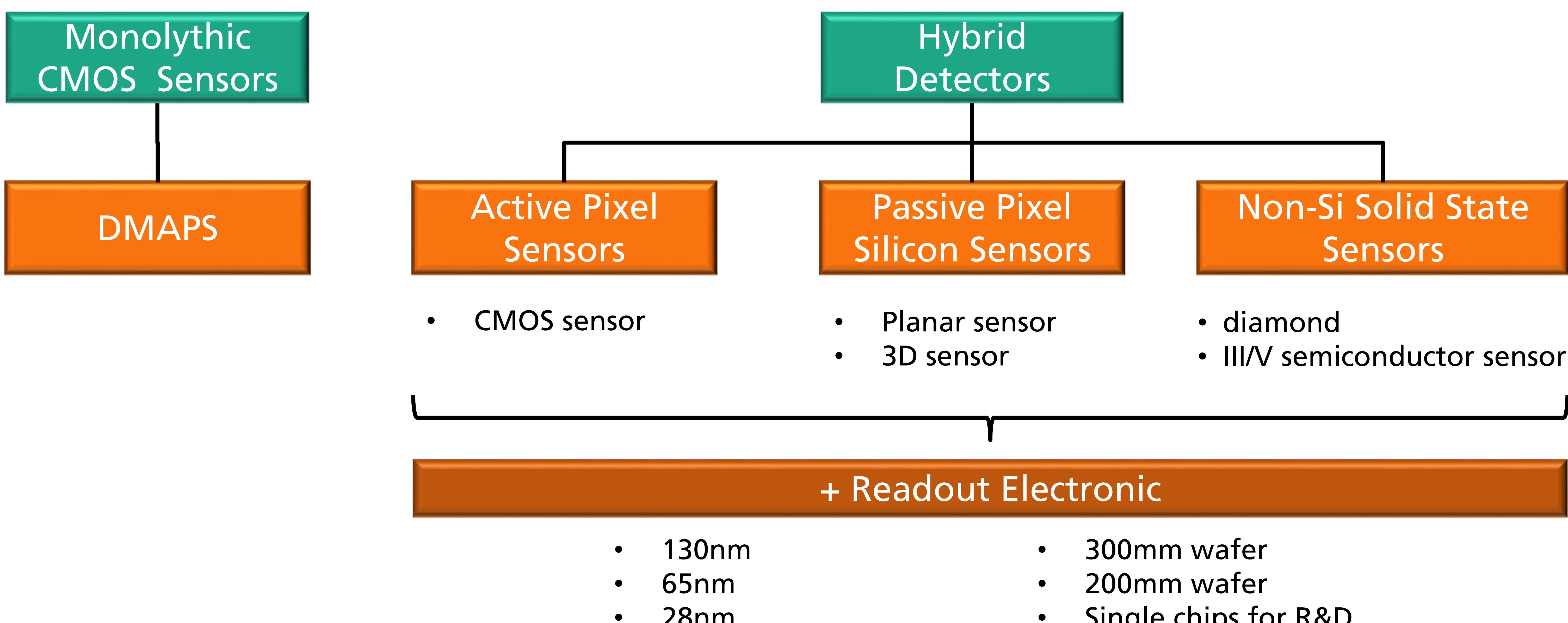
Solid State Sensor Pixel Detector Modules



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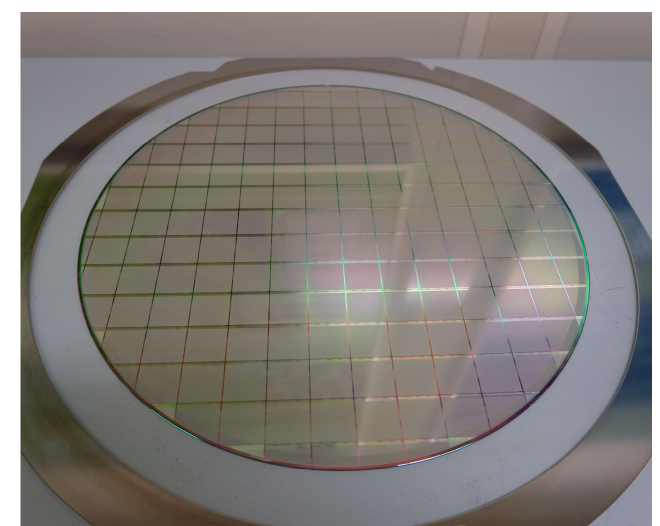
Wafer Substrate Size - Process Line Capabilities

Readout Chip

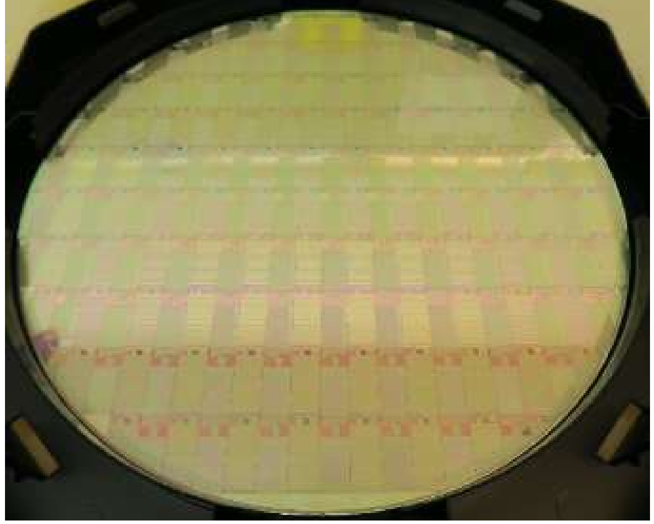
- 300mm wafer, TSMC 65nm technology
- 132 RD53B/ITKPix readout chips per wafer
- Bumping pitch 50x50 µm²
- RD53B: 400x384 bumps (153.600 chip / 20.275.200 wafer)
- 300mm thin wafer handling (≤ 150µm)

Sensor Chip

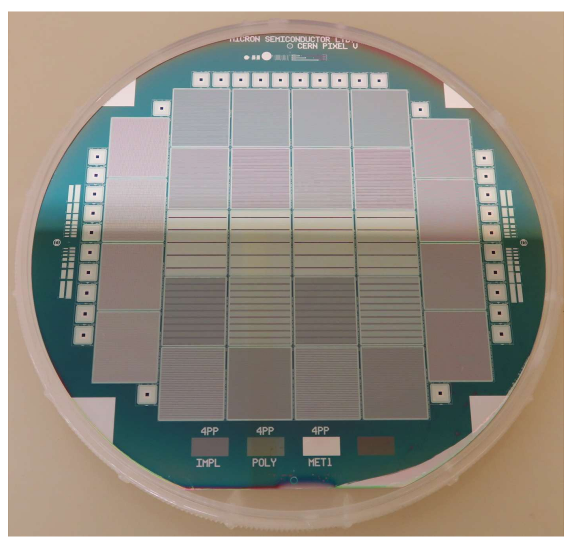
- 150mm sensor wafer: planar or 3D sensor technology
- 200mm CMOS sensor
- UBM deposition process: electro-plating, e-less (NiAu), PVD
- Thin Wafer Handling: 150µm,100µm, 50µm wafer thickness
- Single chip processing with and without carrier



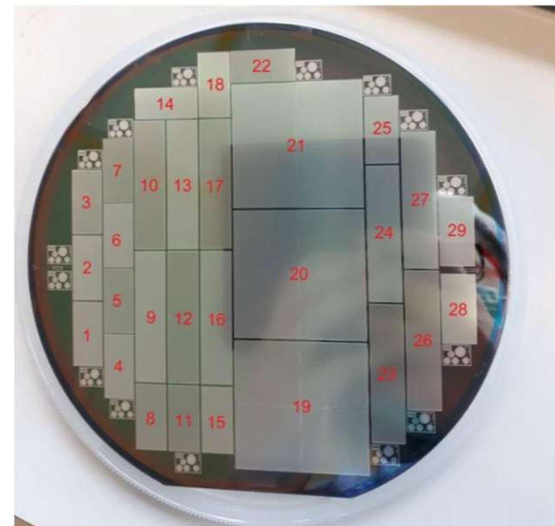
RD53B/ITKPix 300mm ROIC Wafer



RD53A 300mm ROIC Wafer



MICRON planar sensor wafer



FBK planar sensor wafer

Wafer Level Post Processing Line for 150mm, 200mm and 300mm Wafer Size required

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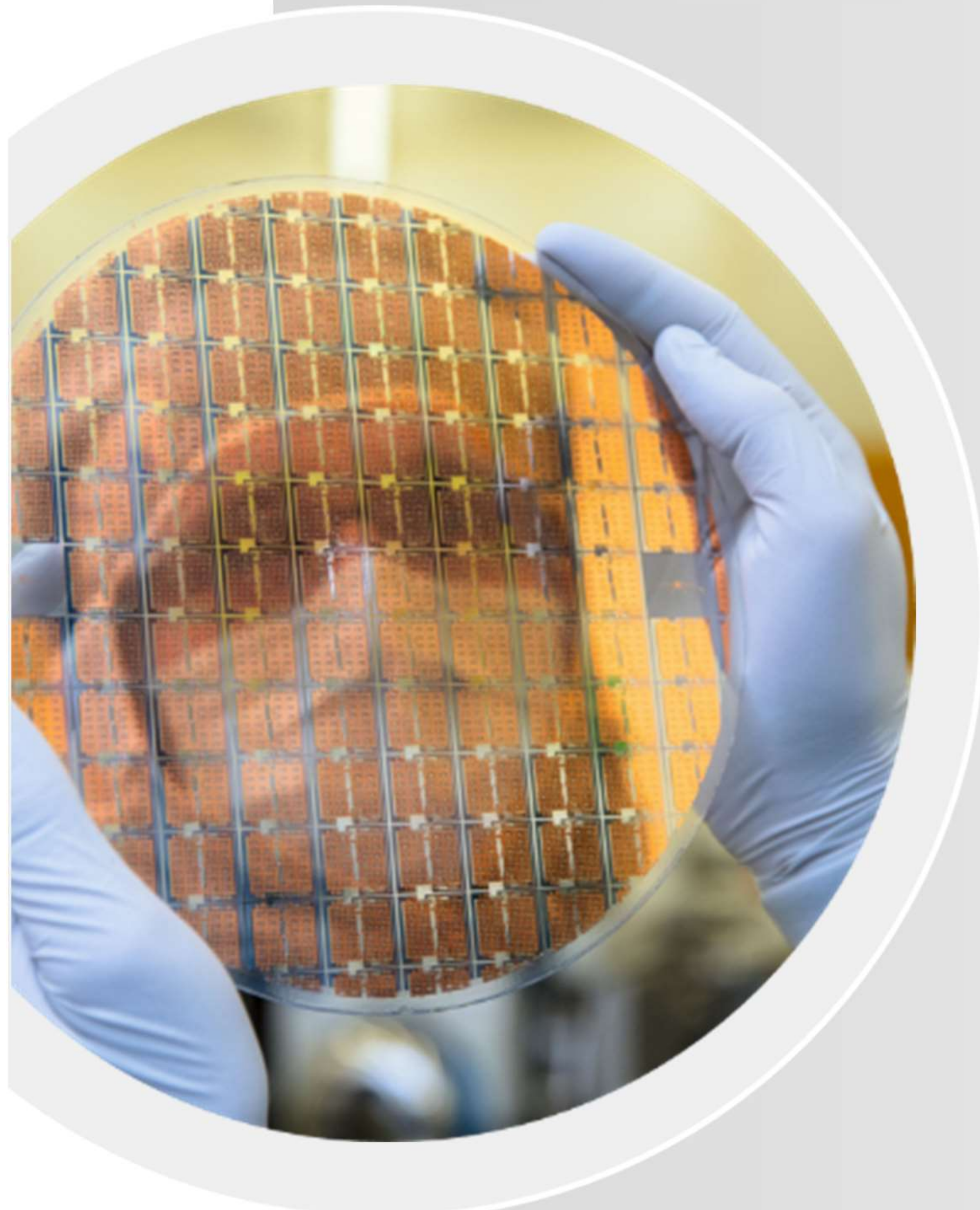
Outline



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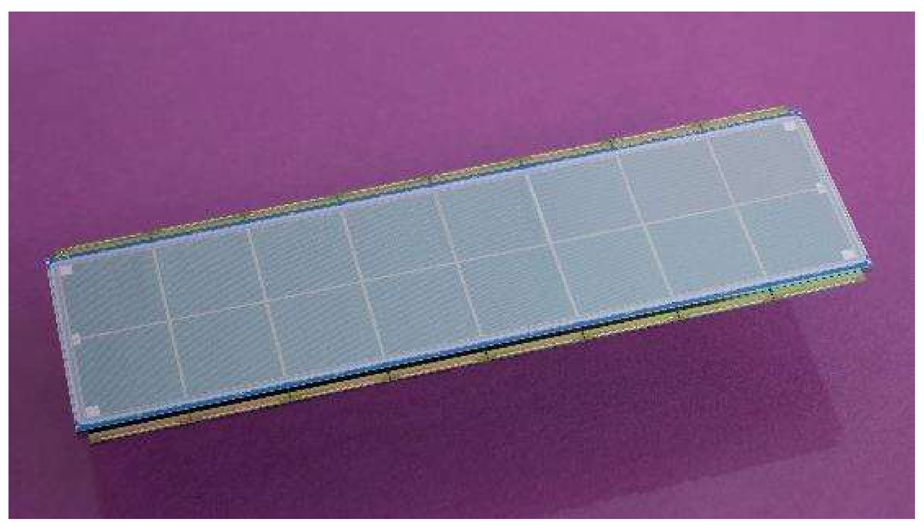
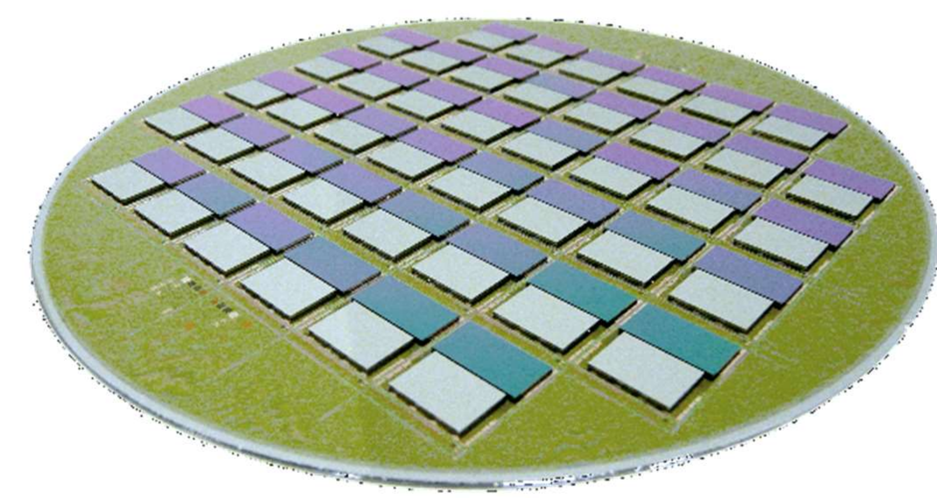
Assembly by Flip Chip Bonding – C2C and C2W



Chip to Wafer



Flip Chip Assembly Bonding Tools:

- High accuracy chip pick and place process ≤ 1μm
- Interconnection by temperature and optionally pressure:
  - reflow soldering
  - thermo-compression bonding,
  - thermosonic bonding

Requirements:

- Chuck size: sensor chip size (~10cm) or wafer size up to 300mm and corresponding working space
- Load station (from dicing frame or from waffle pack)
- Consistent with subsequent dicing process
- Advantage: Chips/wafers with different size and pattern can be merged

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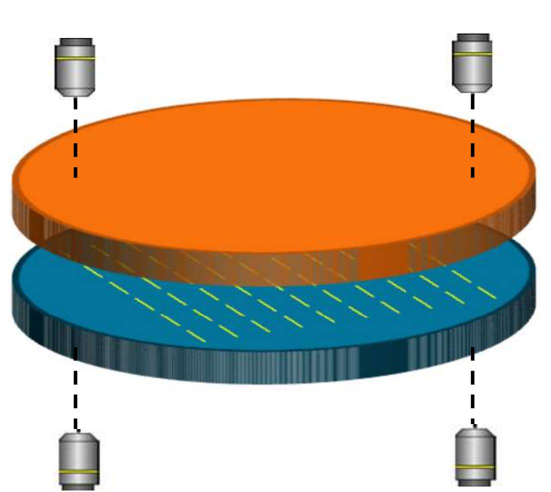
Assembly by Wafer to Wafer Bonding – W2W

Fully/Semi-Automated Wafer Bonder:

- Wafer size 200 mm, 300 mm
- maximum force: 60 kN
- maximum temperature: 550 °C
- vacuum: $1x10^{-5}$ mbar
- Wafer to wafer alignment accuracy <1µm

Applicable Bonding processes:

- Adhesive bonding
- Silicon direct bonding
- Anodic bonding
- Solder/eutectic bonding
- Thermo-compression bonding
- Metal-oxide hybrid boding



Requirements:

- Wafer size matching: top and bottom wafer of the same size
- Design matching: reticle/chip step and repeat; design/wafer origin
- Particle free and planarized wafer surfaces
- Special processes with pre-assembled wafer possible (parallel KGD assembly)
- Consistent with subsequent dicing process

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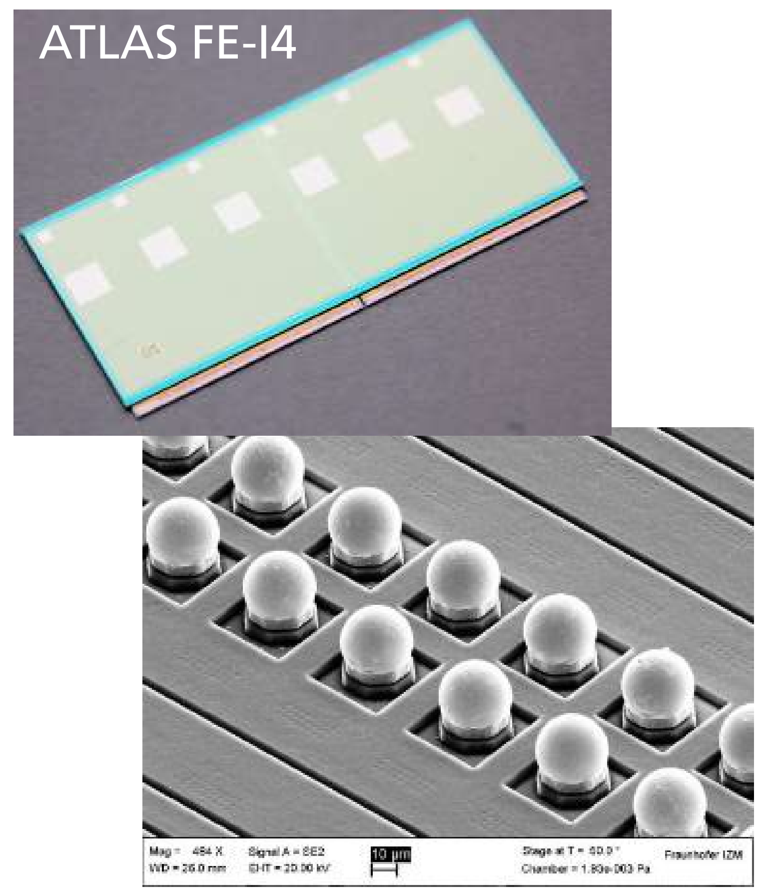
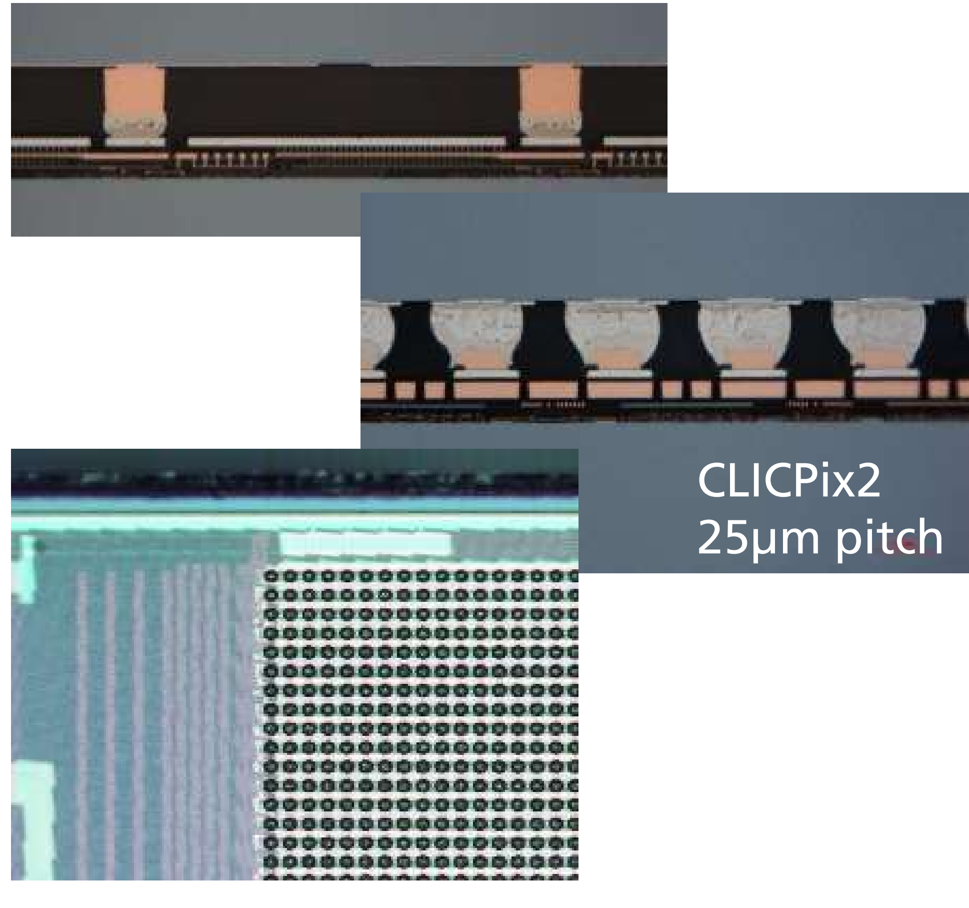
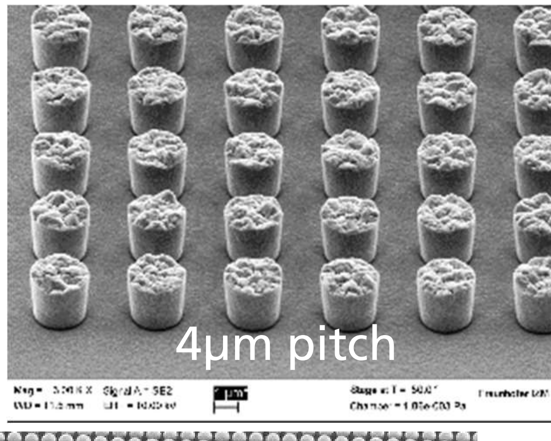
Flip Chip Assembly Key Parameter: Interconnection Pitch

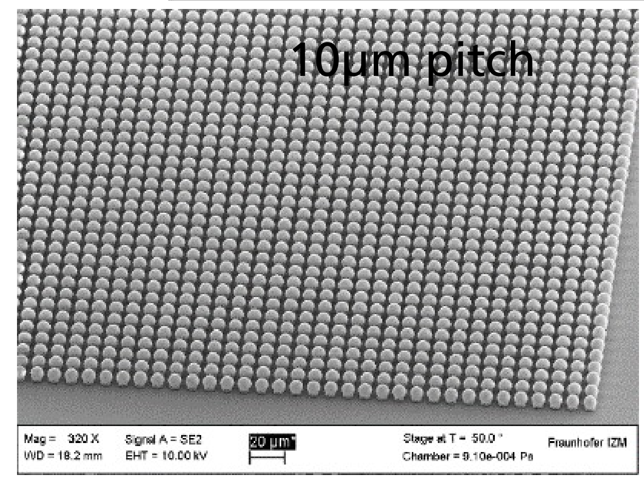


Fine pitch bumping:
Pitch 100…50µm
Bump size: 50…25µm
Material: Solder bumps, pillar bumps with solder cap



µ-bumping:
Pitch 50…20µm
Bump size: 25…12µm
Material: Solder bumps, pillar bumps





Sub-10µ-pitch:
Pitch 10…2 µm
Bump size: 6…1µm
Material: pillar bumps, metal pins

Reduction of pixel pitch – more challenging assembly process

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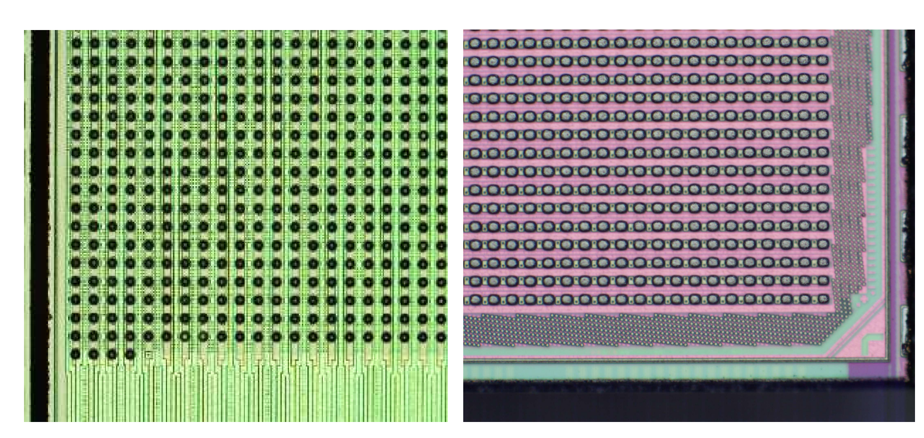
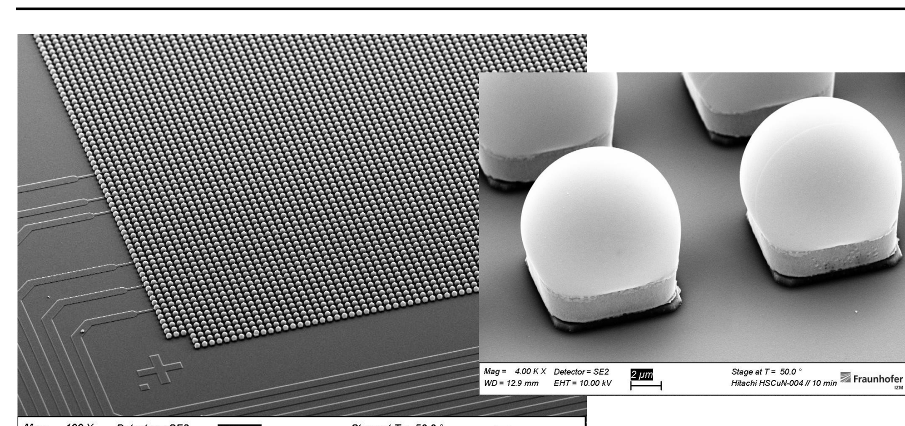
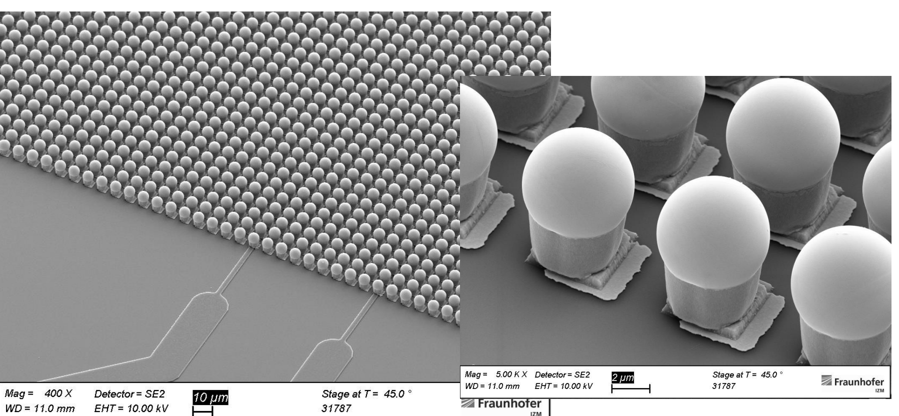
Solder Bump Bonding – Bump Size and Bump Pitch Developments

	Bump pitch	Bump size/material	Wafer size
	RD53/ITKPix: 50µm ClickPix2: 25µm	RD53/ITKPix: 50µm SnAg ClickPix2: 17µm SnAg	300mm TSMC65nm Single chips
	IZM Test-chip: 15µm	IZM Test-chip: 9µm In, SnAg	200mm
	IZM Test-chip: 7.5µm	IZM Test-chip: 4µm In, SnAg	200mm

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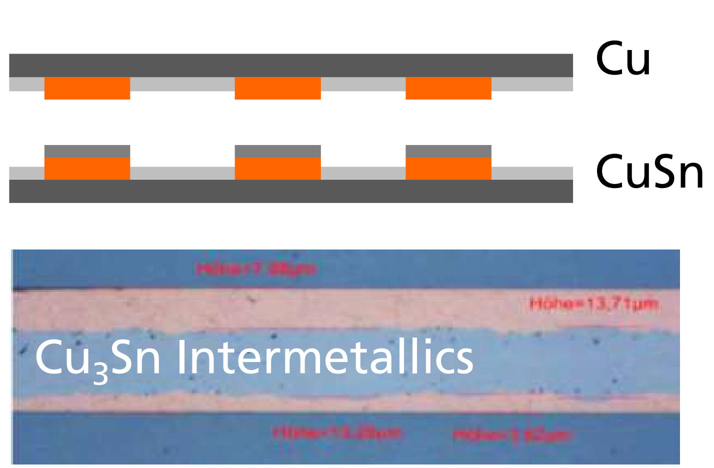
Transient Liquid Phase Bonding (TLPB) / Solid Liquid Interface Diffusion (SLID)



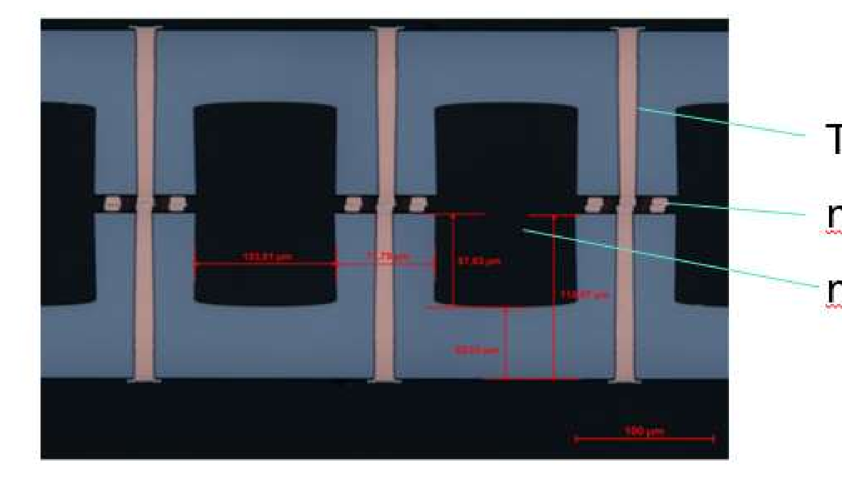
- ECD Cu and Cu-Sn pads
- High melting Cu_3Sn IMC (676°C)
- Bonding parameters:
  220…280°C, 10…50MPa, T= min
- High planarity necessary
- Inert atmosphere required

Hermetic Sealing

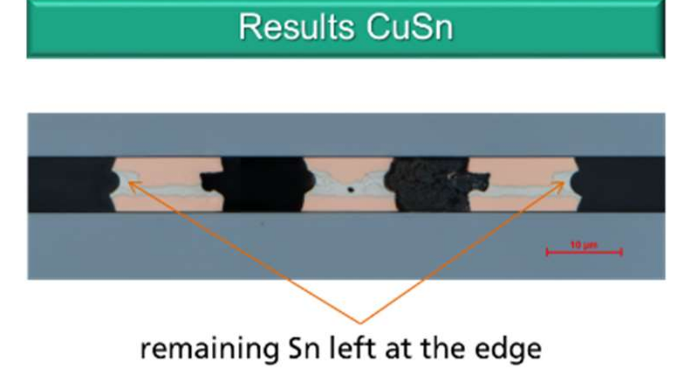
CarrICool

Silicon interposer:
2 half-shells forming a microchannel cooler

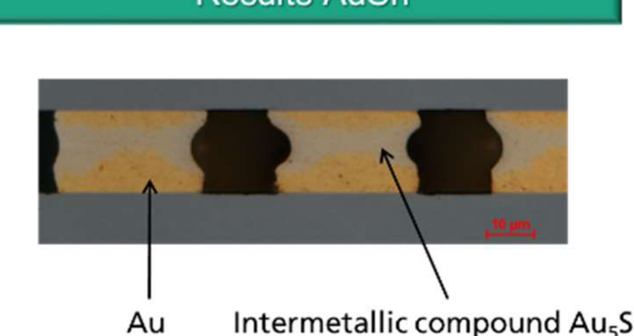
4-port fludic interposer



Results CuSn



Results AuSn



Process available for C2C, C2W, W2W assembly

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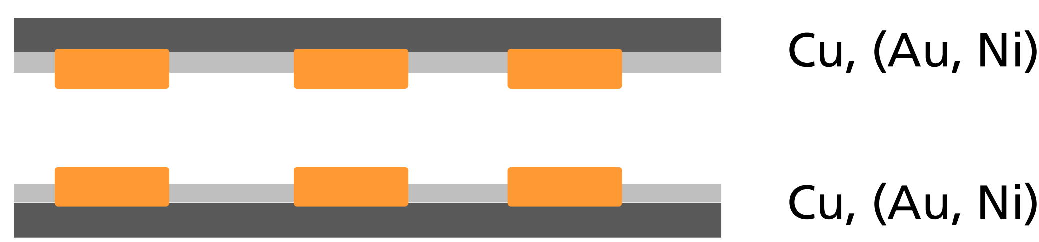
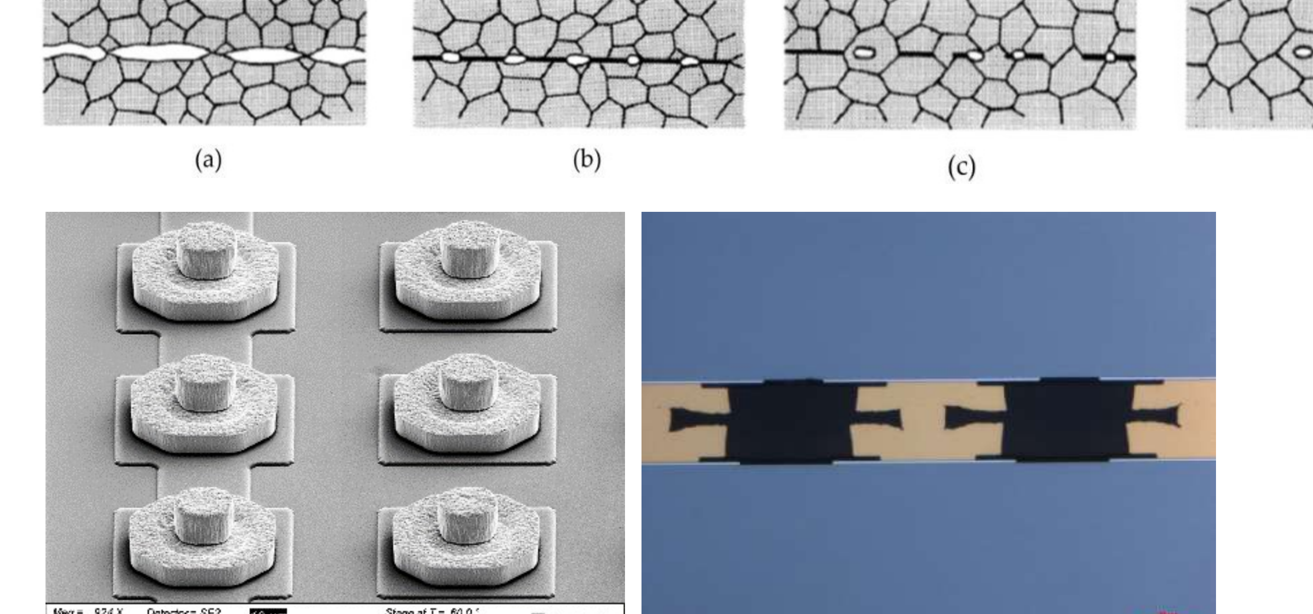
Bonding without Solder: Metal-Metal Diffusion Bonding



- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters:
  - 250°C…400°C,
  - 50…150MPa
  - t= min…h
  - Noble metal contacts or bonding in inert atmosphere
- Interconnection for 3D chip stacking



Au-µ-pillar after metal-metal bonding onto Au pad

Reduction of Bonding Force – MEDIPIX3 size chip 256x256 pads:

- Regular pad size: 30µm, 150MPa → ~7kN bonding force per chip
- Pillar pad: 10µm, 150Mpa → 770N bonding force per chip

Process available for C2C, C2W, W2W assembly

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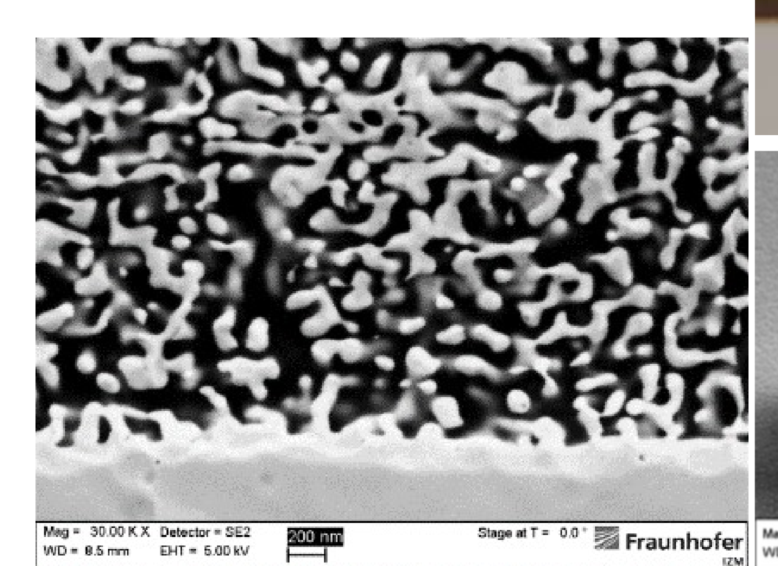
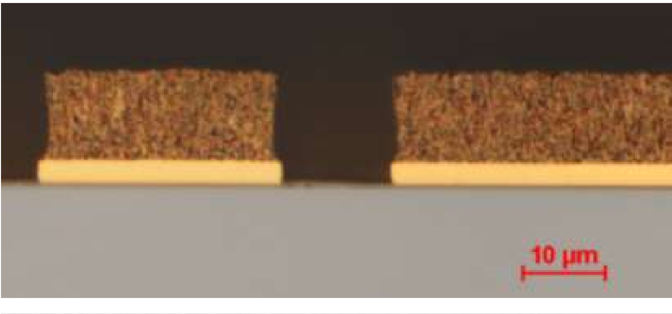
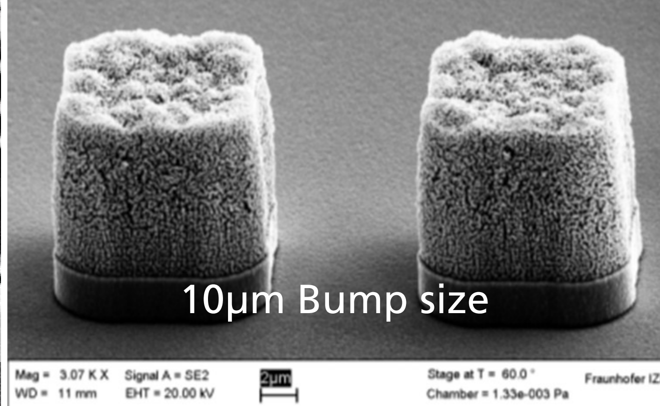
R&D: Nano-Porous Gold (NPG) Bumps for Chip Interconnections

- Development electro-plating baths for Ag/Au alloy deposition
- Prozess flow similar to conventional Au Bumping
- Skeleton formation due to dealloying by wet etching of Ag
- Average pore sizes adjustable from 20 nm up to 500 nm
- TC-Bonding with reduced bonding parameters possible, typ. 10 MPa @ 200°C or 15 Mpa @ 150°C
- Sponge-like Au is fully compressible and able to compensate topography and inhomogeneity on chip and substrate
- Interconnect and pitch size below 10µm possible

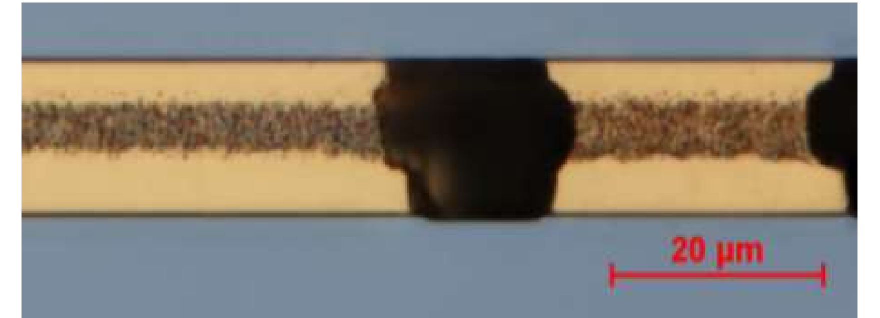
Metal Deposition:

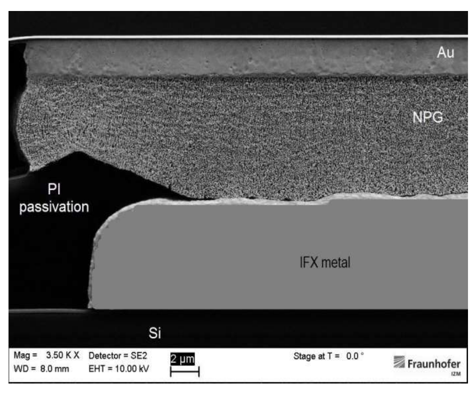






Bonding:





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Bonding without Solder: Metal-Metal Bonding with Anisotropic Conductive Film

Mateus Vicente Barreto Pinto (CERN)
Pixel detector hybridization and integration with Anisotropic Conductive Films
TREDI2021, 16th Workshop on Advanced Silicon Radiation Detectors
Trento, 16-18 February 2021

Process:

- E-less Ni-Au (ENIG) contact pad formation (with / without resist mask) on ROC and sensor wafer
- ACF lamination 50°C … 80°C (polymeric film with metal coated polymer filling particles)
- Flip Chip Bonding with temperature and pressure 150°C … 180°C, bonding pressure depends on IO count

Remarks:

- Interconnect technology for displays (LCD and OLED), camera modules, RFID chips: 25µm pitch range (1D), chip 30x1mm²
- Pressure for high IO counts (ITKPIX >150.000 pixel)
- Long term stability under radiation to be investigated

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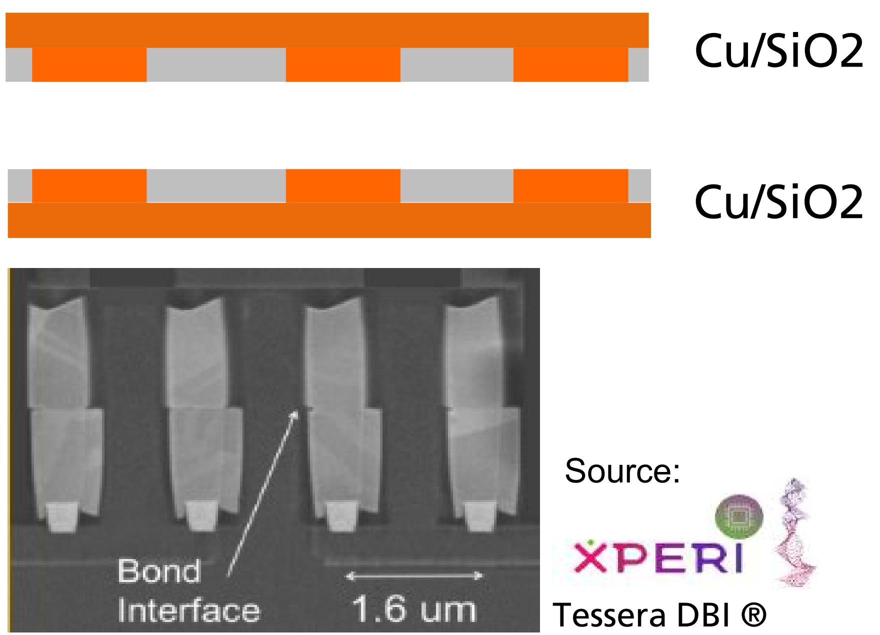
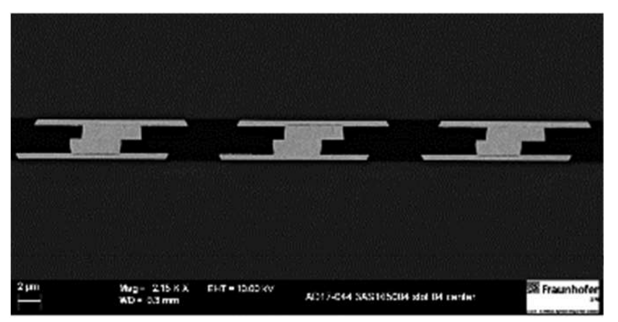
Metal – Oxide Hybrid Bonding

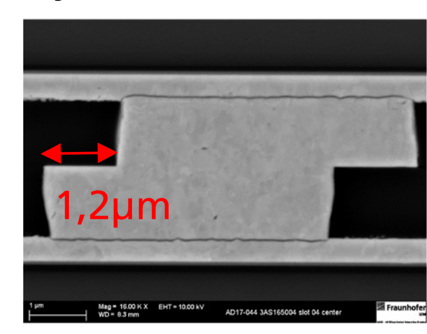


Process:
- SiO2 passivation + Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 150 – 300°C
- 3D chip stacking: memory chips, CMOS image sensors (CIS)

Motivation for DBI®:
- W2W , D2W, D2D
- Highest interconnect density: I/O pitch down to 1 µm
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- High reliability

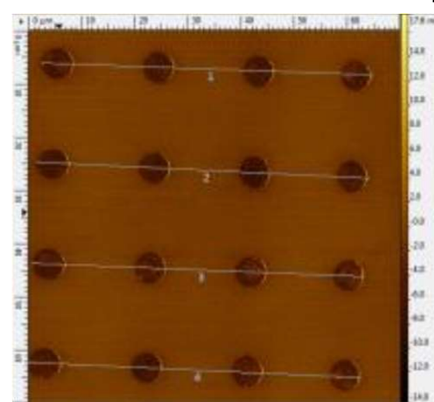
Fraunhofer IZM-ASSID: 300mm W2W Bonding with <5µm alignment accuracy





J. Wolf „3D System Integration Requirements and Potential Solutions", European 3D Summit, 22-24.1.2018, Dresden, Germany.

Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%



	FhG IZM ASSID (Results)
Roughness beside TSV (Oxide) Ra	0,146 nm
Roughness on TSV (Cu) Ra	0,163 nm
Planarization	5nm @ 100µm

Surface preparation in nanometer range → Atomic force microscopy

Processes patented, licence required for Invensas ZiBond® direct bonding, DBI® and DBI Ultra hybrid bonding technologies

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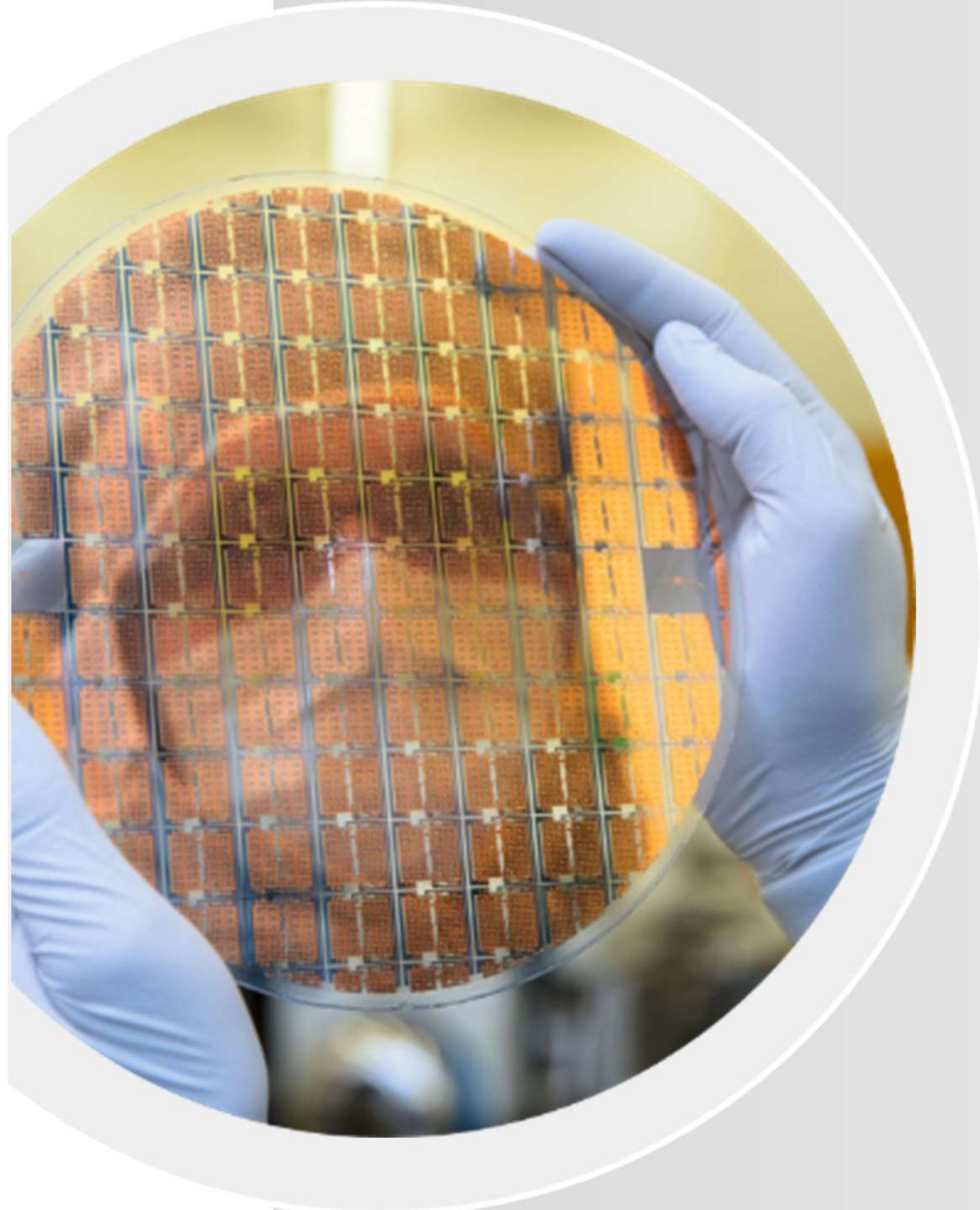

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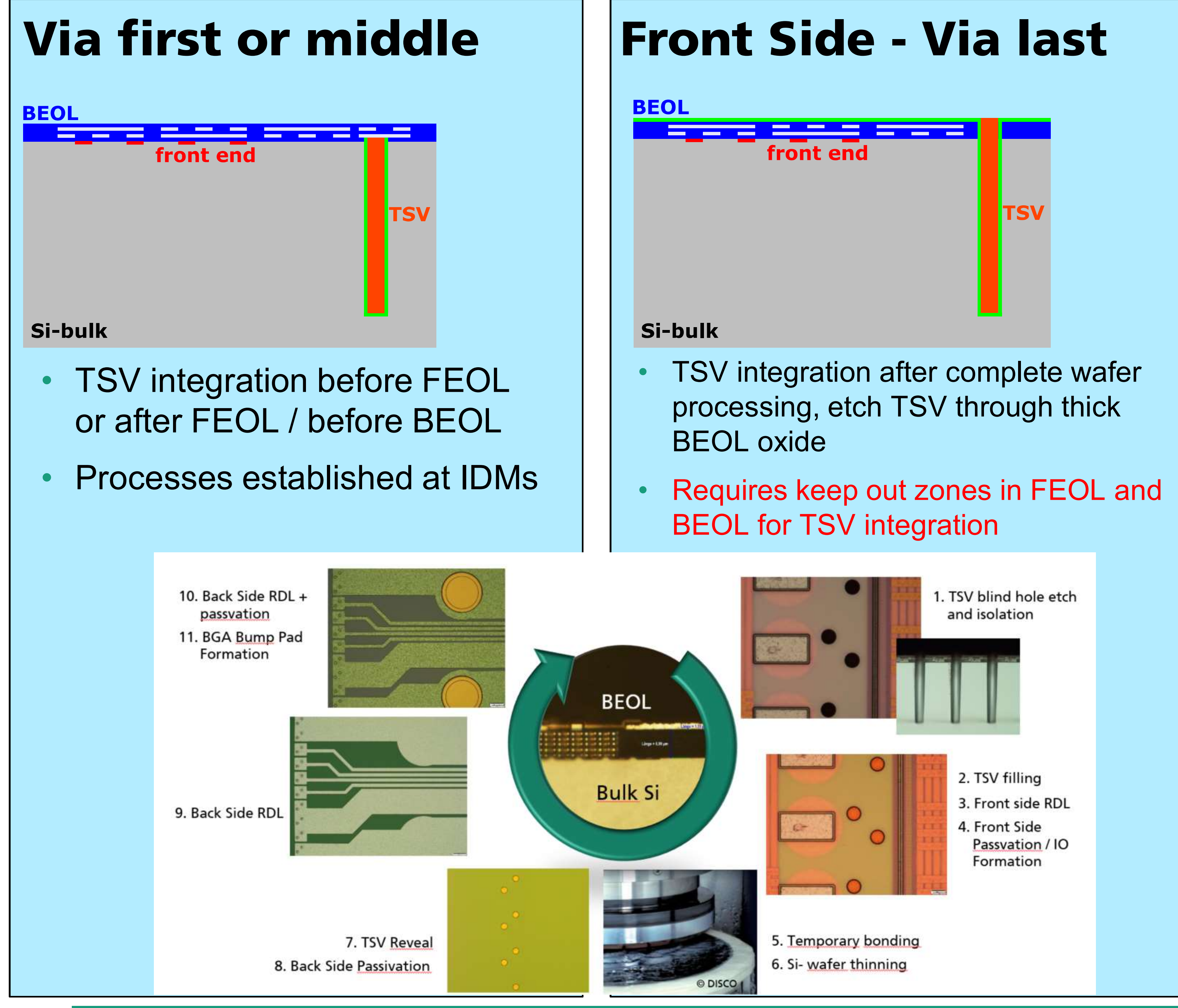
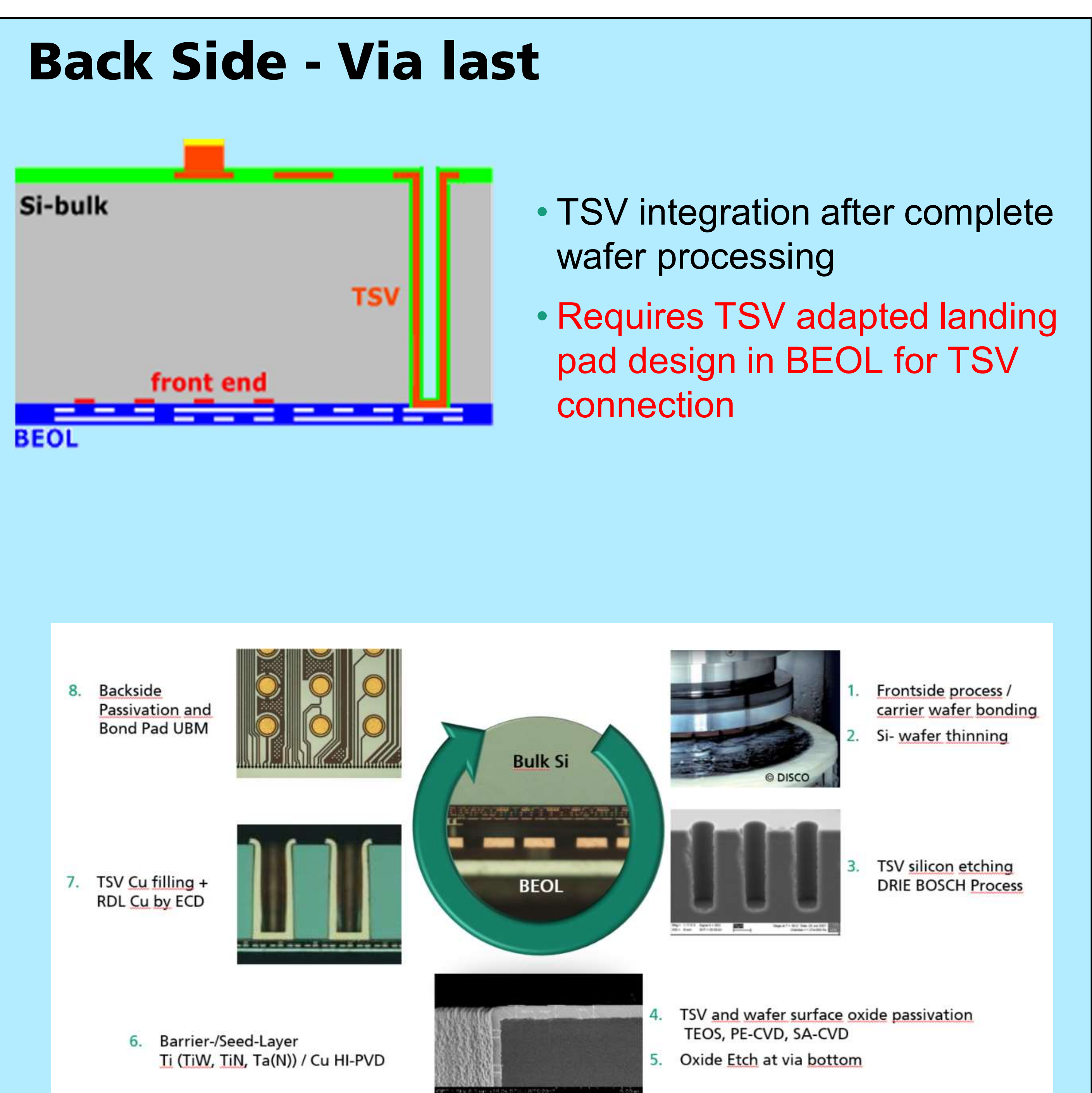
TSV Integration Schemes





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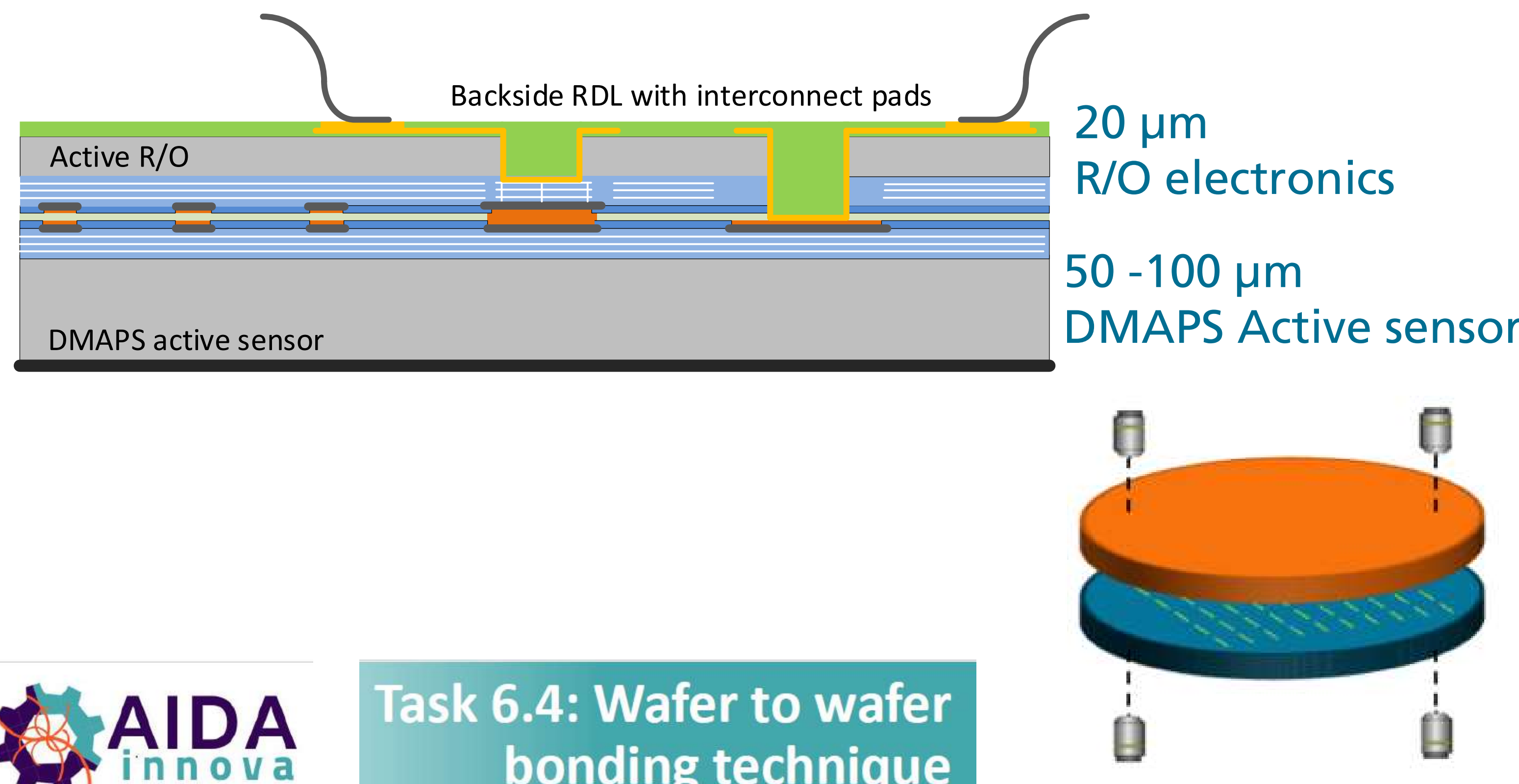
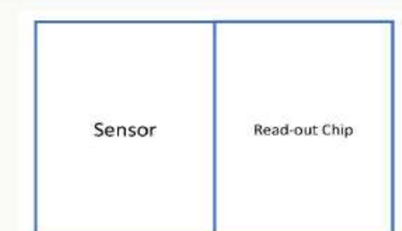
Ultra Thin Hybrid Pixel Detectors

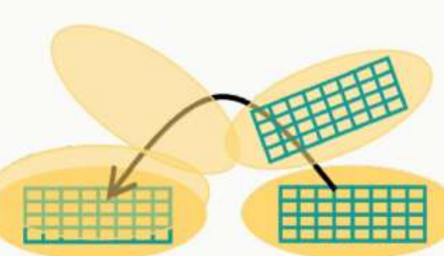
- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer with backside via last interconnection
- Bonding layer with metal-metal or capacitively coupled contacts
- Thin DMAPS sensor with contact pads and backside processing



Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:

- Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
- Use either TimePix3 chip wafers (130 nm on 200 mm wafers) or own FE development on the same wafer as the sensor
- Develop and optimize hybridization process including thinning and interconnection from chip's backside
- Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics (long term, not with AIDAinnova)





This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

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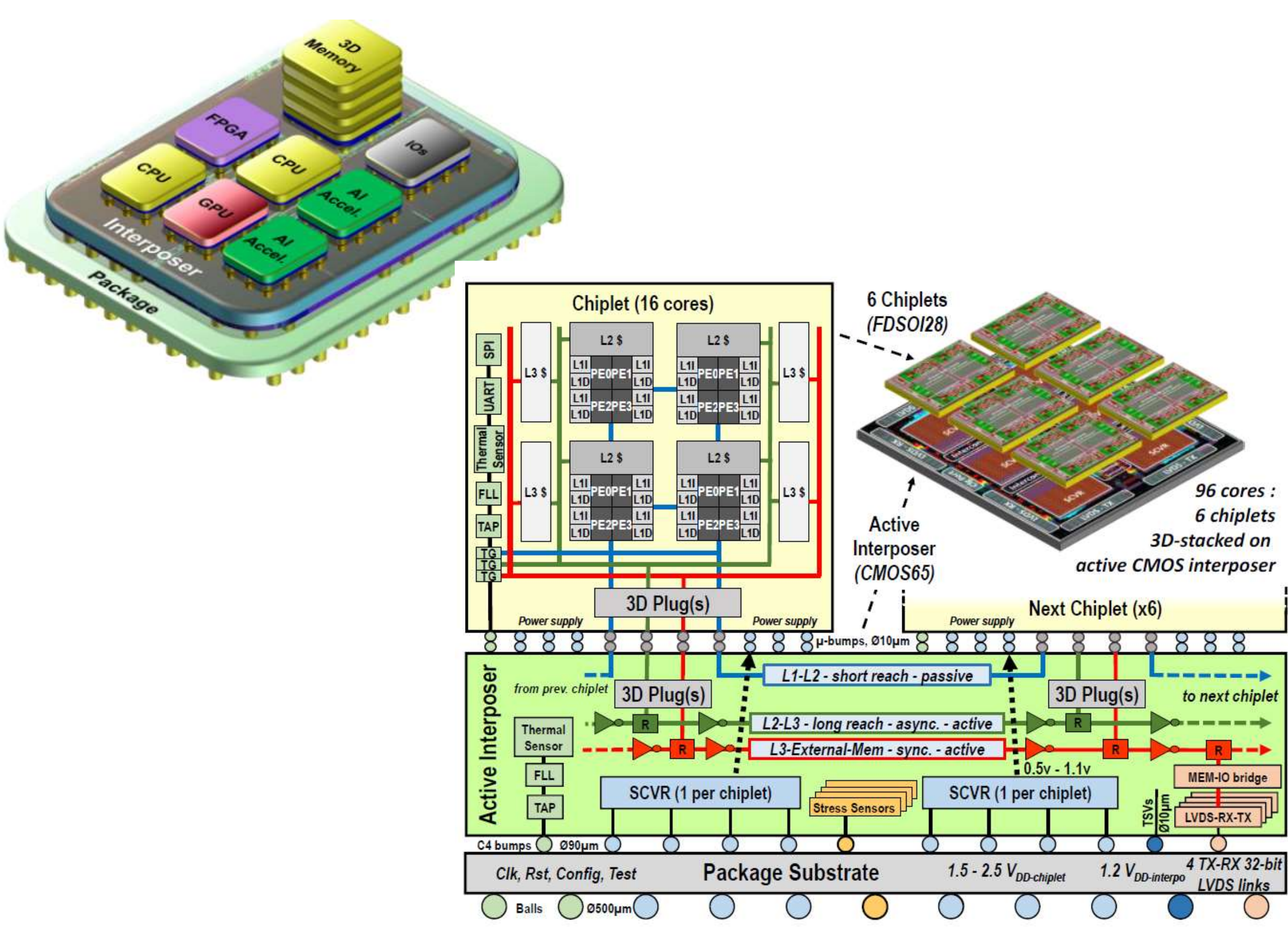
Industry Technology Trend: Processor Chiplet Assembly on Active Interposer



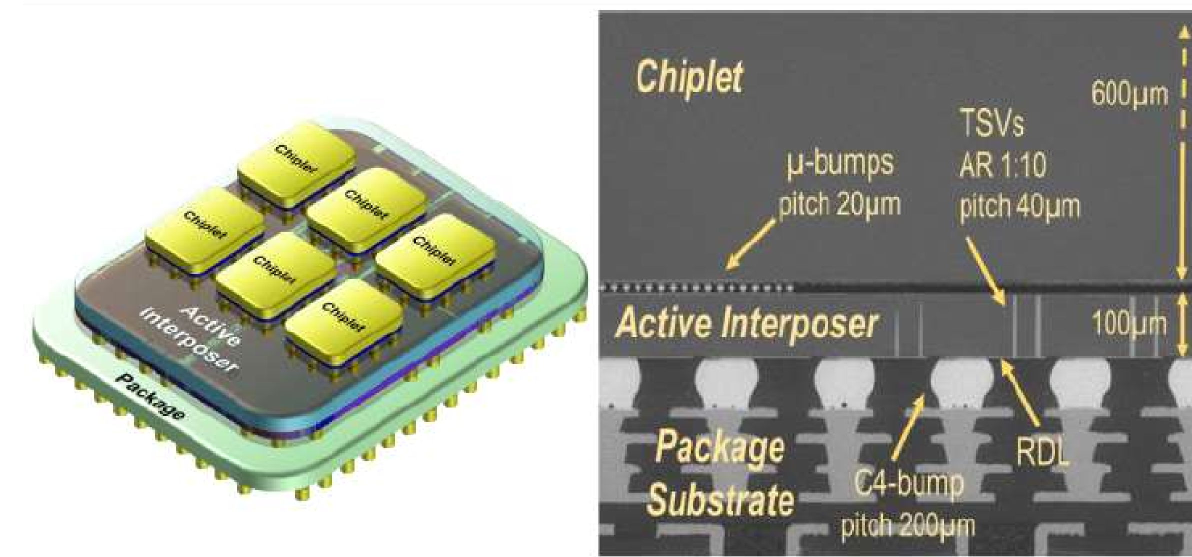


Fig. 5. INTACT : from concept to 3D-cross section

TABLE I: INTACT MAIN CIRCUIT FEATURES AND 3D TECHNOLOGY DETAILS

Chiplet technology	FDSOI 28nm, 10 metals, 0.5V-1.3V+adaptive biasing
Chiplet area	4.0 mm x 5.6 mm = 22.4 mm^2
Chiplet complexity	395 Million transistors, 18 transistors/µm^2 density
Interposer tech.	CMOS 65nm bulk, 7 metals, MIM option, 1.2V
Interposer area	13.05 mm x 15.16 mm = 197.8 mm^2
Interposer complexity	15 Million transistors, 0.08 transistors/µm^2 density
3D technology	Face2Face, Die2Die assembly onto active interposer
µ-bump technology	Ø10µm, pitch 20µm
#µ-bumps	150 000 (20k signals + 120k powers + 10k dummies)
Inter-chiplet distance	800µm
TSV technology	TSV middle, Ø10µm, height 100µm, pitch 40µm
#TSV	14 000 TSV (2 000 signals + 12 000 power supply)
Backside RDL	10µm width, 20µm pitch
C4-bumps	Ø90µm, pitch 200µm, 4,600 bumps
Flipchip package	BGA 39 x 39, 40mm x 40mm, 10 layers
Balls	Ø500µm, pitch 1mm, 1 517 balls

Pascal Vivet, Eric Guthmuller, Yvain Thonnart, Gaël Pillonnet, Cesar Fuguet, et al.. IntAct: A 96-Core Processor With Six Chiplets 3D-Stacked on an Active Interposer With Distributed Interconnects and Integrated Power Management. IEEE Journal of Solid-State Circuits, Institute of Electrical and Electronics Engineers, 2020, pp.1-1. 10.1109/JSSC.2020.3036341 . hal-03072959

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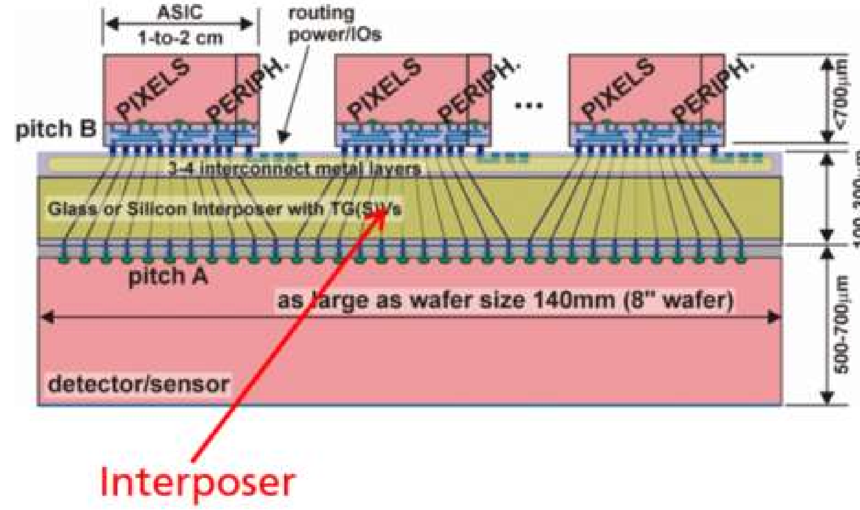
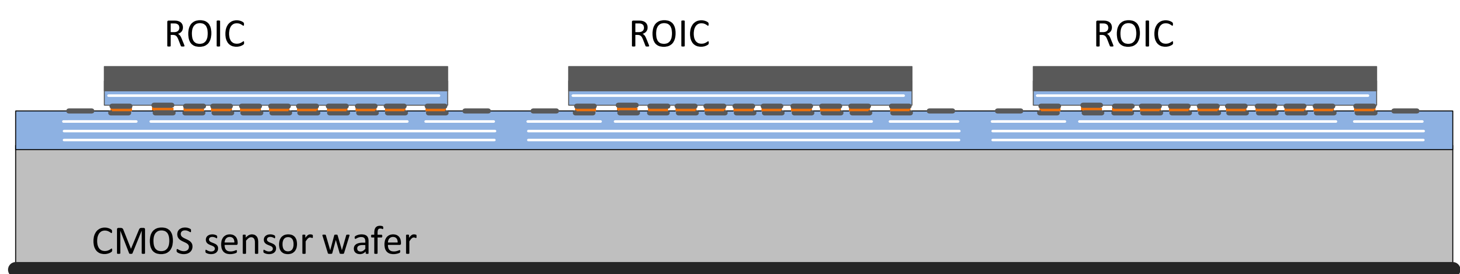
Concept in HEP: CMOS Sensor Interposer

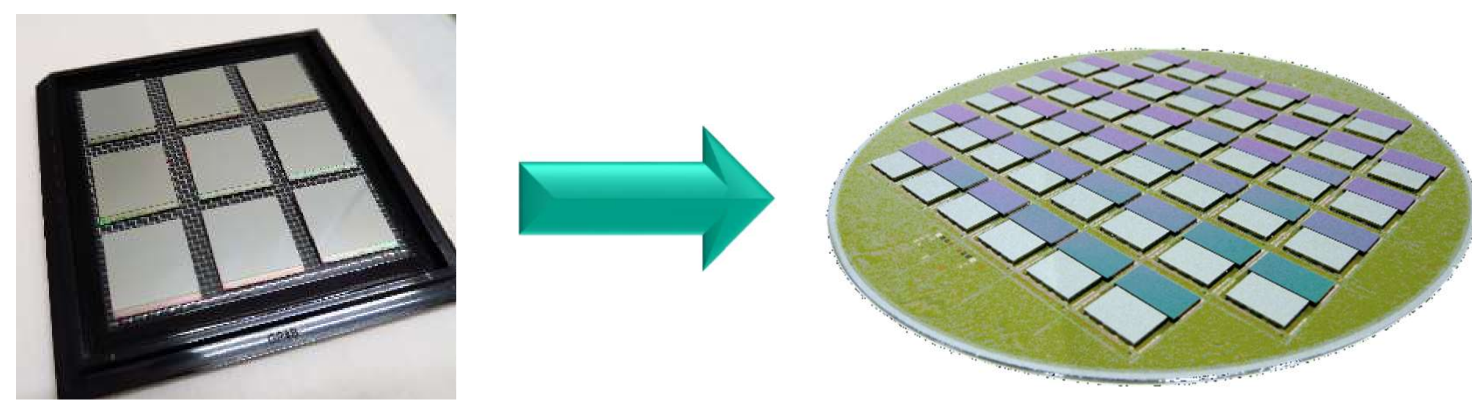
Concept presented by Grzegorz Deptuch, Fermilab, CPIX 2014:



- Readout chips bonded onto Si/Glas Interposer top side with bumping pitch B
- Sensor bonded onto interposer bottom side with pitch A
- Interposer to sensor W2W bonding possible
- ROC assembly by C2W bonding possible



- Readout chips bonded onto sensor wafer with BEOL RDL and bonding pads
- Readout IO contact pad fan-out RDL on sensor top metal layer
- Connection to module support flex via bond pads on sensor
- optional ROCs with TSV first or middle → reduce post processing steps
- C2W assembly → sensor chip has to be slightly bigger than ROC



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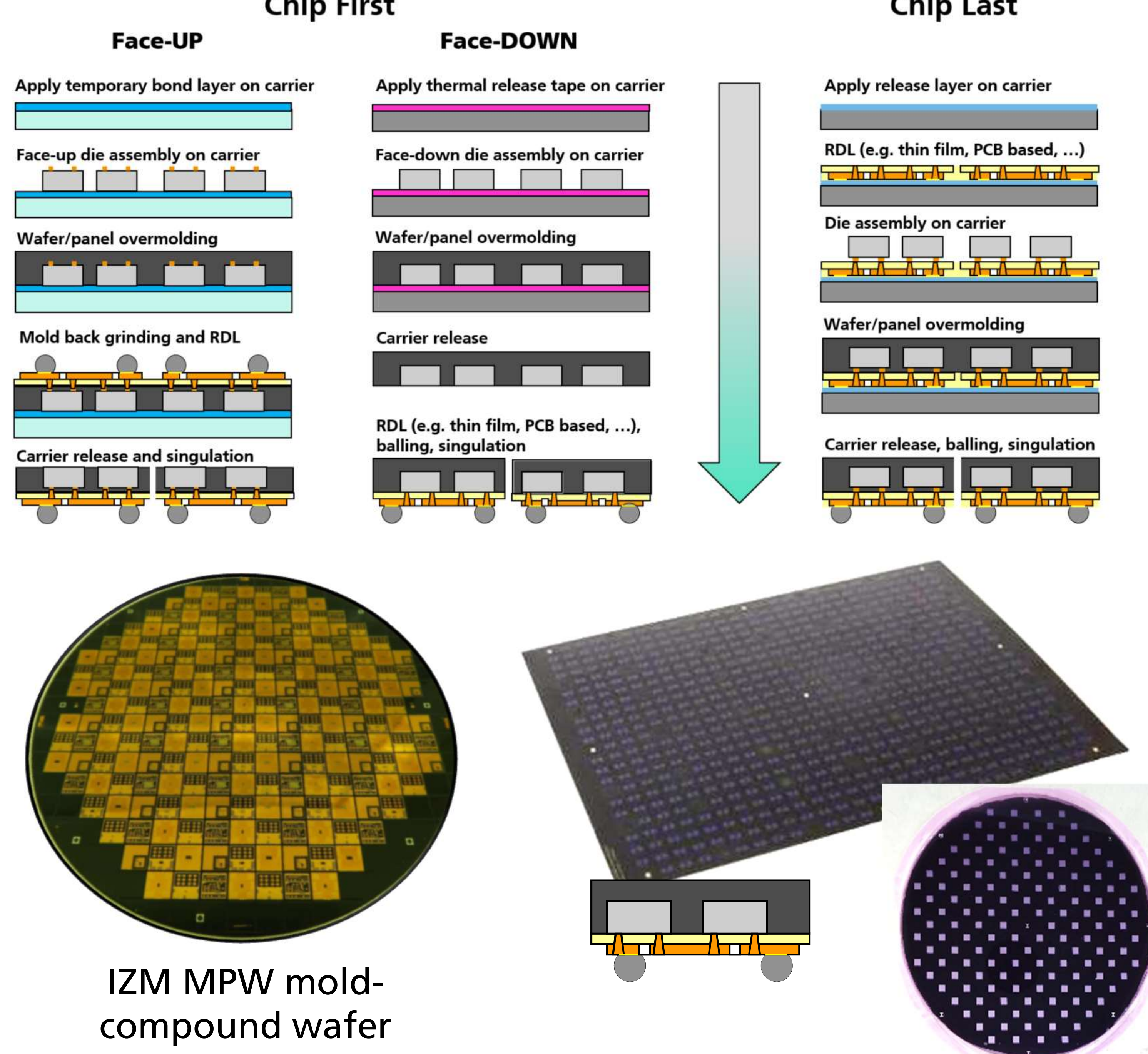
Industry Technology Trend: Embedding and Fan-Out Wafer Level Packaging



IZM MPW mold-compound wafer

- KGDs embedded in a mold-compound on 200mm, 300mm wafer level or panel level
- Thin film post processing at wafer or panel level
- Chip IOs connected via thin film fan-out RDL, in most cases for SiP assembly onto PCB
- Thinning and dicing using regular post processing equipment and processes

Possible benefits for HEP:

- Can be used for serial powering?
- pre-assembled stave-structures?
- Others?

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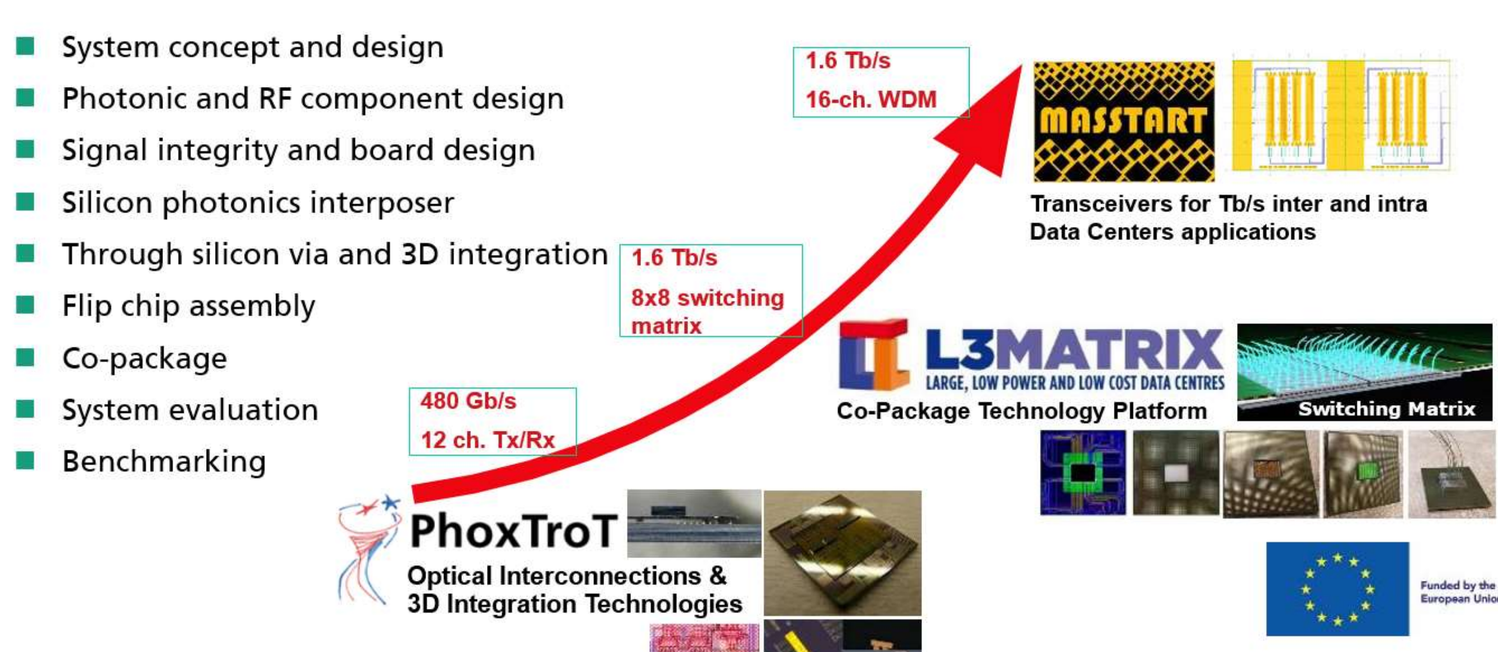
Industry Technology Trend: Photonic Integration Technology

Empowering Photonic Interconnects for Data Center and NGC



photonic interposer | photonic components | ASIC | glass substrate | 1000 µm | photonic interposer | glass substrate | ASIC | photonic interposer | ASIC | ASIC | TSV | TSV | Switching Matrix

Source: www.PhoxTroT.eu

Source: www.L3matrix.eu

- High data rate communication using Photonic IC (PIC)
- Drivers in Industry: next generation computing - cloud, edge, node HPC
- Electrial and optical integration on silicon photonic interposer and PIC
- Optical off-chip interconnection for chip-to-chip communication: low-latency, high-bandwidth, high density, low power
- Massive switching beyond 400 Gb/s with new developed Serializer/Deserializer cicuits and optical links

Tolga Tekin, Fraunhofer IZM

New technological paths for high performance chips targeting HPC and edge, EXDCI Workshop, Brussels, 05. - 06.11.2019

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Conclusions

- 65nm and 28nm readout electronic chips will be produced on 300mm wafer:
  → requires 300mm post process line for R&D and production - 2D only or fully equiped 3D line?
  → MPW single chips: post processing for R&D
- Sensor wafer 100mm? – 150mm – 200mm wafer size:
  → additional post processsing line for these wafer sizes
  → diamond sensor: single chip post processing?
- Ultra thin wafer handling:
  → 100µm…50µm..20µm with temporary/permanent carrier concepts
  → 150mm, 200mm, 300mm wafer size
- Concepts for C2W and W2W hybridization:
  → start this already at design level
  → keep it simple, more reticle stepper pattern than „pizza“ design
- Different bonding processes are available for C2C, C2W and W2W:
  → some restrictions in availability due to patent protection
- Adaption of trends from industry for integration technologies, i.e.
  → chiplet stacking
  → embedding and fan-out packaging
  → photonic packaging

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