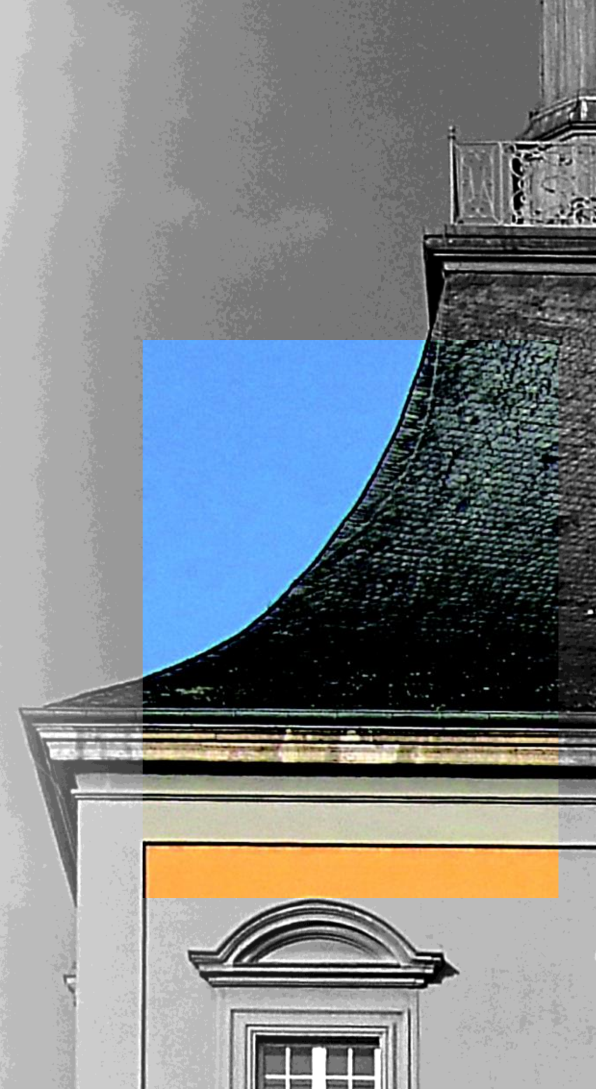
UNIVERSITÄT BONN

SI LAB Silizium Labor Bonn

PASSIVE CMOS SENSORS

IN 20 YEARS...

ECFA 2021



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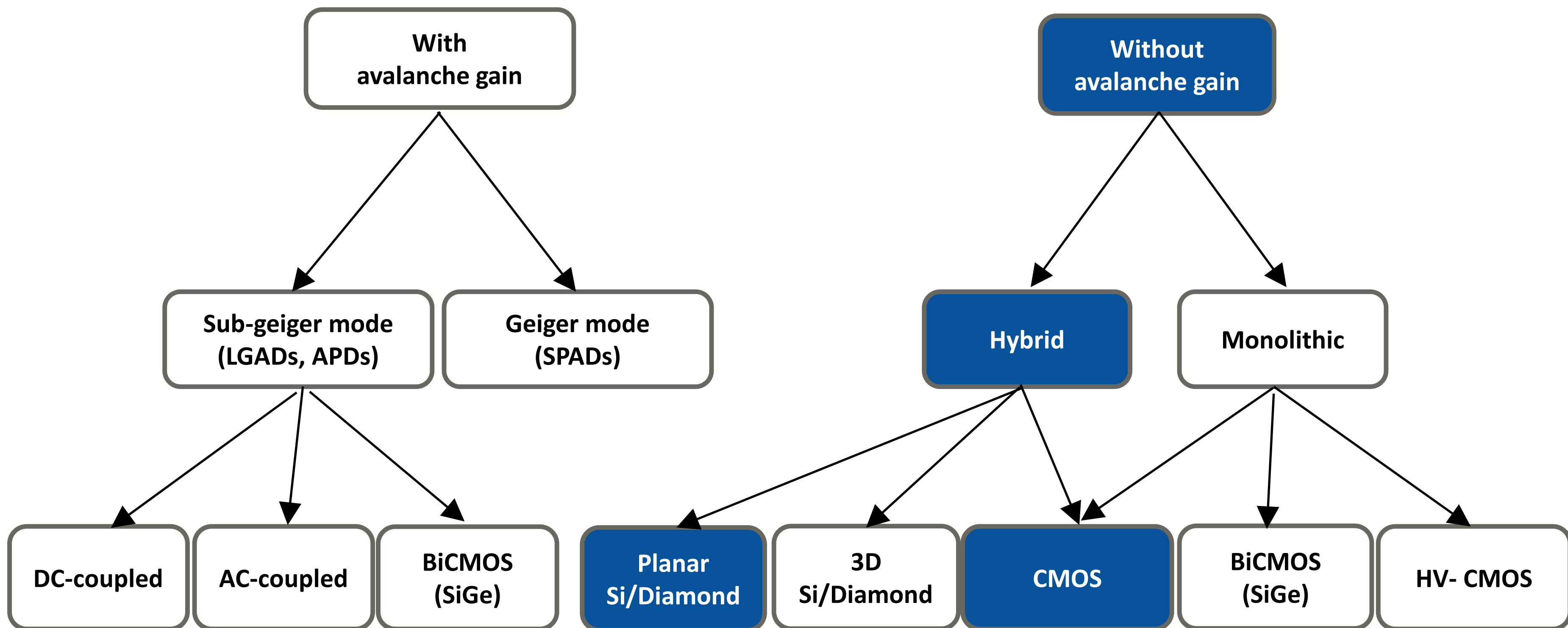
David-Leon Pohl

SOLID STATE DETECTORS FOR FUTURE (4D) TRACKERS



OUTLINE

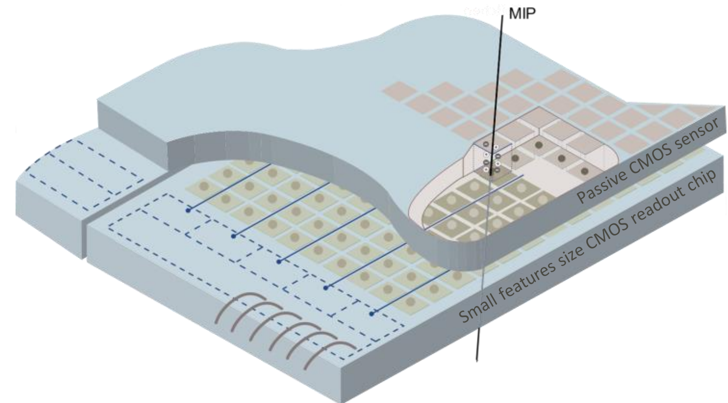
1. Introduction
    - What are „passive“ CMOS sensors?
    - Benefits and challenges
2. Status
    - History
    - Passive CMOS sensors for silicon trackers at the HL-LHC-pp
3. Outlook & Summary

PASSIVE CMOS SENSORS

- Current situation:
  - Full-wafer lithography with 150 mm wafers for passive sensors in silicon tracking detectors (CMS/ATLAS)
  - Area of silicon tracking detectors is increasing
  - ➔ Increasing demand for large-scale sensor wafer production
  - Only few large-scale suppliers available
  - Risk: single-vendor scenario
  - Some investigations into 200 mm wafer processes for silicon sensors, e.g.:
    - Silicon strip tracker: 10.1016/j.nima.2018.06.069
    - CMS High Granularity Calorimeter

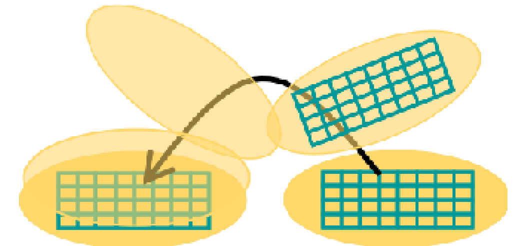
Idea:

- Use a CMOS processing line on large, high-resistivity wafers (kΩ-cm)
- N-well/p-well/metal layers for sensor implantations and biasing
- No active components ➔„passive CMOS“
- Stitching over reticle boundaries for large sensor tiles



PASSIVE CMOS SENSORS: CHALLENGES AND BENEFITS

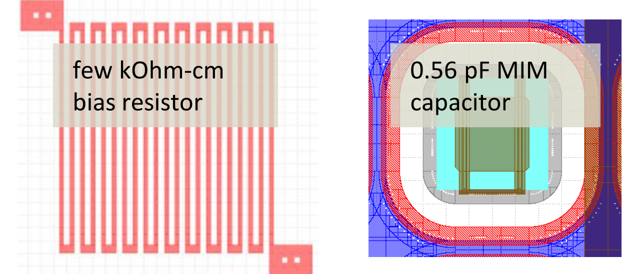
- Find interested CMOS foundry:
  - Mainly of interest for the foundry, if a large production run is at the horizon
  - Good feedback on design helpful (some design rules might be violated)
- Fast production, cheap large-scale production, expensive engineering runs:
  - MPWs allow for design optimizations with small prototypes (guard rings, implant geometry, ...); custom HR substrates sometimes not available for MPWs
  - Engineering runs required (with minimum batch sizes) to develop large sensor tiles and production processes (stitching, back-side processing, thinning, dicing)
- Possible cost reduction: current hybrid pixel costs: 50% hybridization, 40% sensors, 10% readout chip; sensors 3-4 times cheaper
- Easier access to wafer-scale industrial processes, due to wafer size ≥ 200 mm, e.g.:
  - Thinning without handling wafer (TAIKO process)
  - Wafer-to-wafer bonding ➔ ultra-thin low-cost hybrid pixels?



PASSIVE CMOS SENSORS: CHALLENGES AND BENEFITS

- Risk that process is not available after some time (company changes philosophy)
  - Less worrying, since integration density is not as important as for active sensors/RO electronics
    ➔ Many companies to select from (AMS/TSI, ESPROS, LFoundry, TowerJazz, Toshiba, XFAB, ...)
  - Most design rules are not relevant for the large structures of a sensor (usually no need for fine-pitch patterning)
  - Design tools and PDK for the process are available and ease design
  - Porting a design to a new process is not too difficult
    ➔ Time scale ~ 1 month
  - Developing a new large passive sensor (incl. few iterations; back-side processing): 1 - 2 years
- Enhance sensor design using CMOS process features:
  - Poly-silicon resistors → connection to a bias grid
  - MIM capacitors for AC-coupling → no leakage current into readout
  - Many metal layers for redistribution

Resistor / Capacitance in a 50 µm x 50 µm pixel

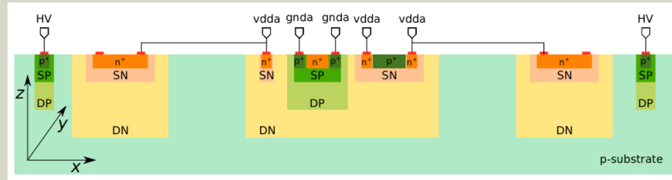


PASSIVE CMOS SENSORS: BYPRODUCT OF DMAPS EFFORTS

(Passive) Test structures

- Test structures / passive diode arrays in many CMOS processes produced, e.g.:

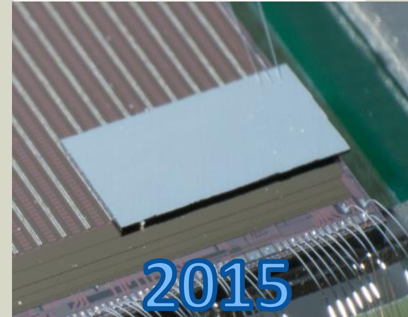
H35Demo test structure



  - AMS 180/350 nm HV-CMOS
  - LFoundry 150 nm CMOS
  - TowerJazz 180 nm CMOS
  - XFAB 180 nm SOI CMOS
- Different substrates investigated
- Varying designs: guard rings, pixel isolation, implantation geometries

Hybrid pixel prototypes

Prototype on ATLAS FE-I4

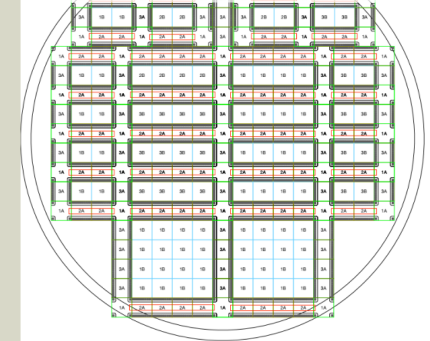


Prototypes on RD53A

Full size, large sensors

- First dedicated submission for vendor qualification for ATLAS/CMS
- „Full-size" pixel sensors and strip sensors

Single, dual, quad pixel module and strip sensors



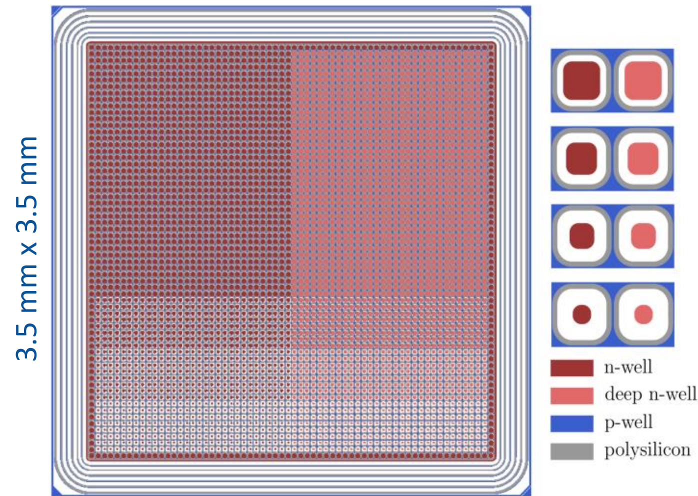
2020

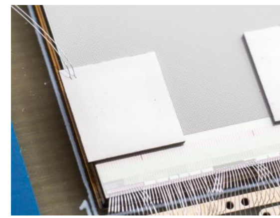
Byproducts of DMAPS efforts

Dedicated submission

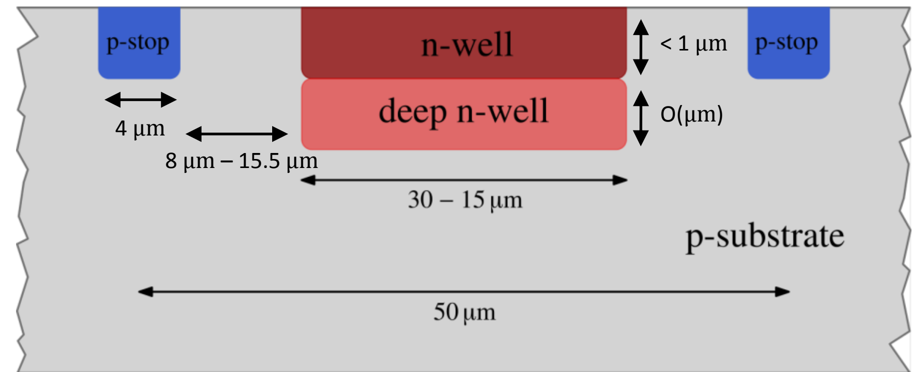
SMALL PROTOTYPE

- High resistivity 4-5 kΩ cm p-type CZ wafer
- 50 µm x 50 µm pixels in 64 × 64 matrix
- 100 µm thickness with TAIKO thinning
- Bump bonded to RD53A
- DC coupled pixels:
  - No biasing structure
  - Variation of implantation width: 15 µm - 30 µm
  - Variation of n-well depth: n-well (NW) and deep n-well (DNW)
- More info in: https://doi.org/10.1016/j.nima.2020.164130



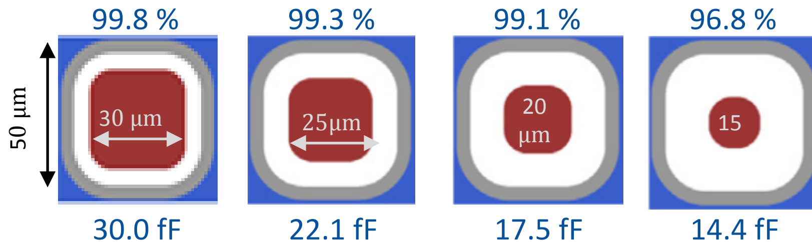


Pixel

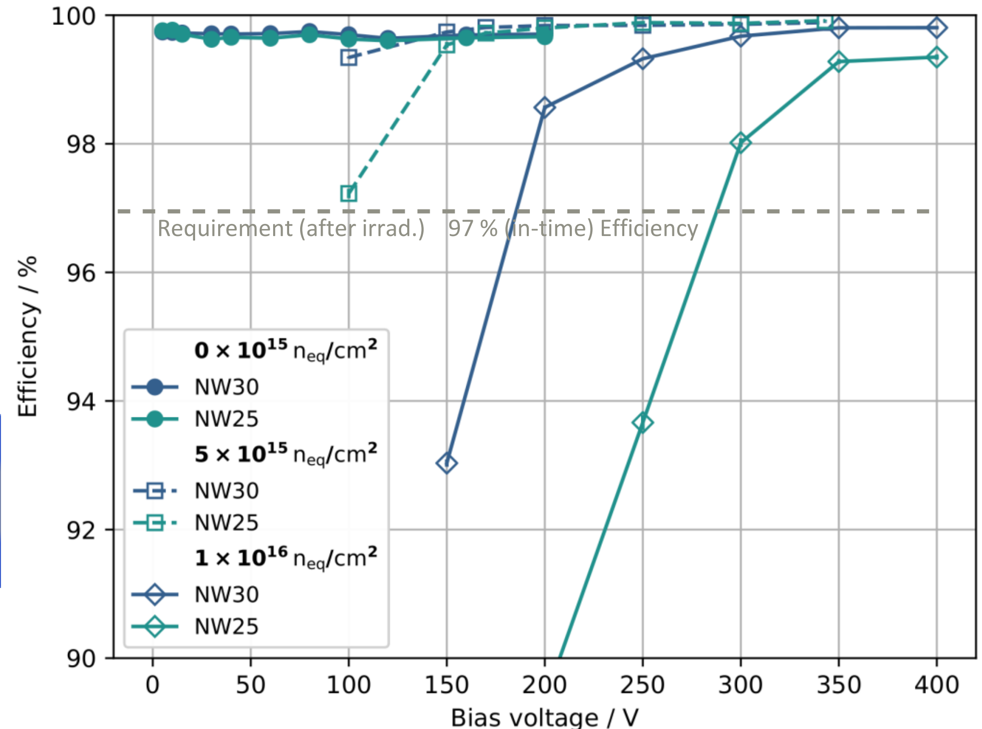


EFFICIENCY MEASUREMENT: PIXEL SENSOR

- R/O chip parameters:
  - Linear FE of RD53A
  - Threshold: ~1000 e
  - Noise occupancy: < 10^{-6}
- Before irradiation: > 99.5 % at 5 V only
- $5 \times 10^{15}\ n_{eq}/cm^2$: > 99 % efficiency (@ 100 V)
- $1 \times 10^{16}\ n_{eq}/cm^2$: > 99 % efficiency (@ 400 V)
- Mean efficiency and capacitance for different fill-factors @ 400 V:



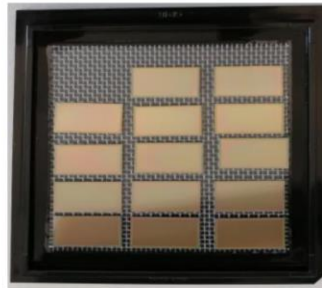
- Capacitance measurement in: https://doi.org/10.1088/1748-0221/16/01/P01029



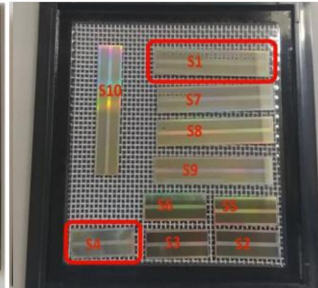
FULL-SIZE PASSIVE CMOS SENSOR SUBMISSION

- Goal: qualify a CMOS vendor for the production of (pixel-) sensors for ATLAS/CMS
- Design:
  - Up to full-size 4 x 4 cm^2 pixel sensor tiles
  - Compatible with RD53 R/O chip development
  - Different pixel flavors:
    50 x 50 μm^2, 25 x 100 μm^2; AC or DC coupled, biasing with > 4 kOhm poly-resistor)
  - Strip sensors: > 4 cm; 75.5 um pitch
  - Float-zone wafer material
  - LFoundry 150 nm 1.8V CMOS process
- Optimization for production:
  - Thinning to 150 µm with handling wafer, backside implantation @ CMOS fab
  - Backside Al-Si metal, UBM, Flip-chip @ ATLAS ITk hybridization vendor

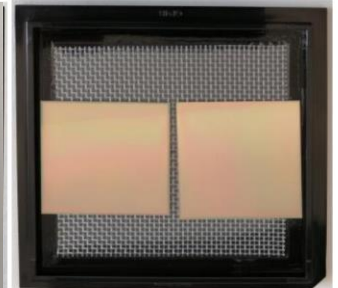
Pixel sensors



Strip sensors



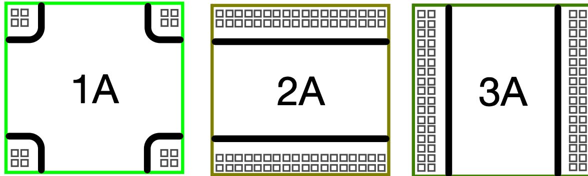
„Quad" pixel sensor



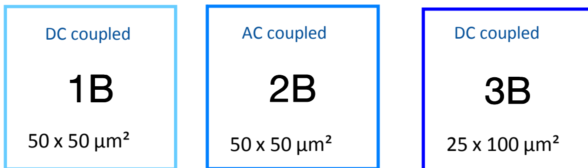
STITCHING

- Sensor size > reticle size
  → Stitching needed
- Additional rules for stitching (no fine-pitch)
  → Not too relevant for sensor designs
- Different blocks:

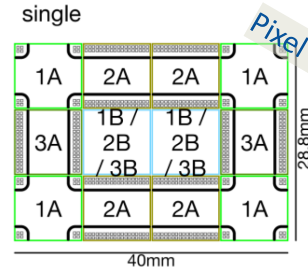
Edge blocks with guard rings, strip sensors and test structures

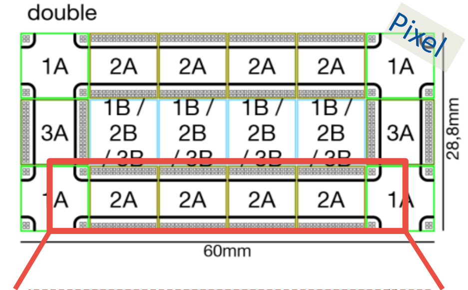


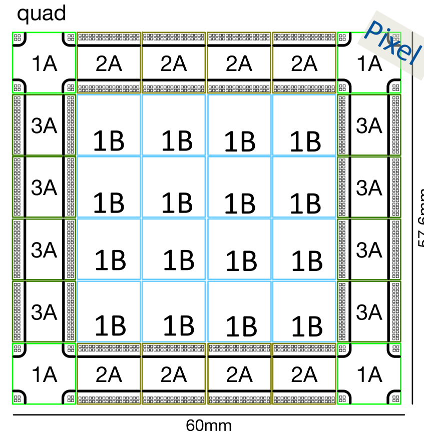
Center blocks with different pixel flavors

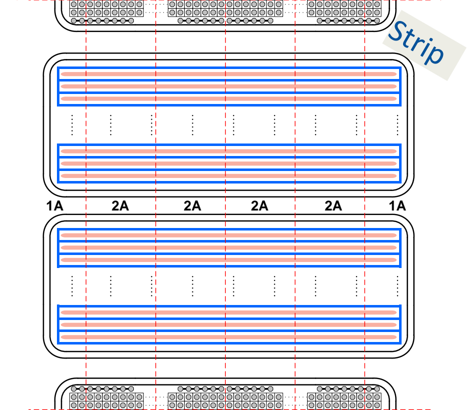


- Different configurations possible
  → arrange and repeat blocks in different order



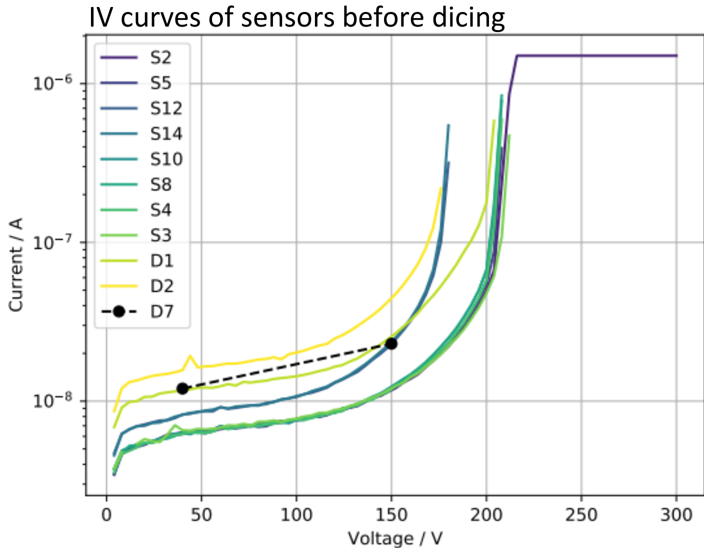






IV CURVES

- Sensor requirements for HL-LHC matched



IV curves of pixel assembles before and after irradiation

Maximum allowed leakage current after 5e15

Maximum allowed leakage current after 2e15

Maximum allowed leakage current before irradiation

0x1B24, DC 50x50 (bare sensor)
0x1B24, DC 50x50 (assembled)
0x1B36, DC 50x50 (bare sensor)
0x1B36, DC 50x50 (assembled)
0x1B25, AC 50x50 (bare sensor)
0x1B25, AC 50x50 (assembled)
0x1153, AC 50x50 (assembled)
0x1B24, DC 50x50 (5e15)
0x1B25, AC 50x50 (2e15)
0x1B36, DC 50x50 (2e15)
0x1153, AC 50x50 (5e15)

10^{2} 10^{1} 10^{0} 10^{-1} 10^{-2} 10^{-3}

Leakage current / $\mu A/cm^2$

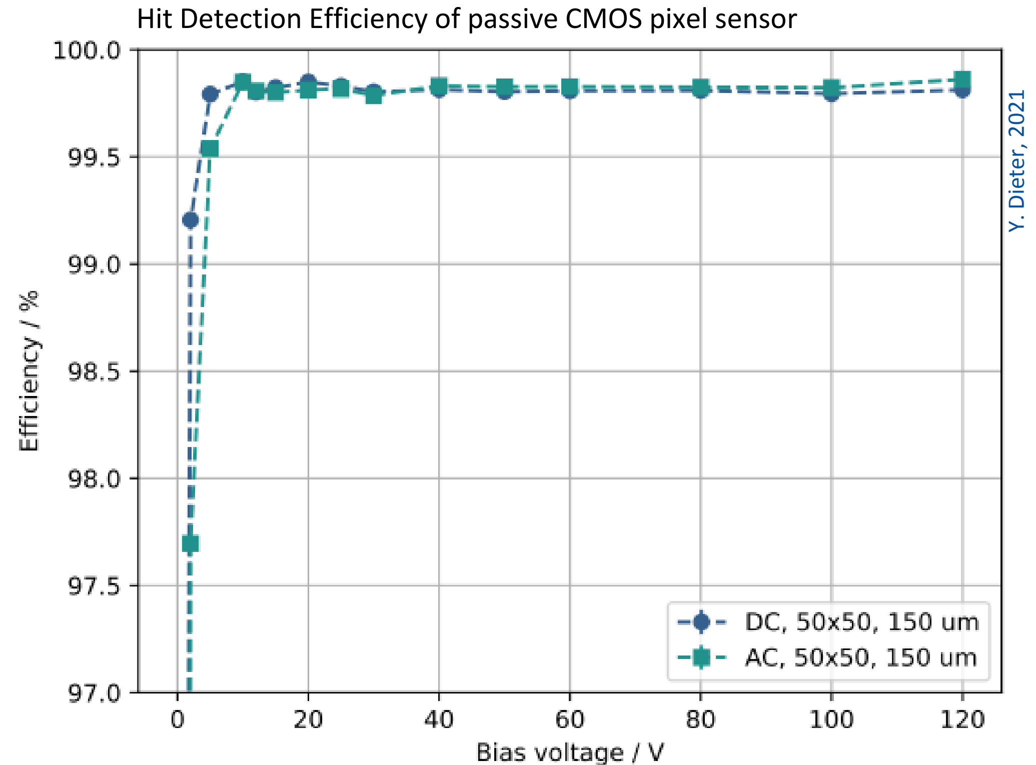
0 50 100 150 200 250 300 350 400

Voltage / V

Y. Dieter, 2021

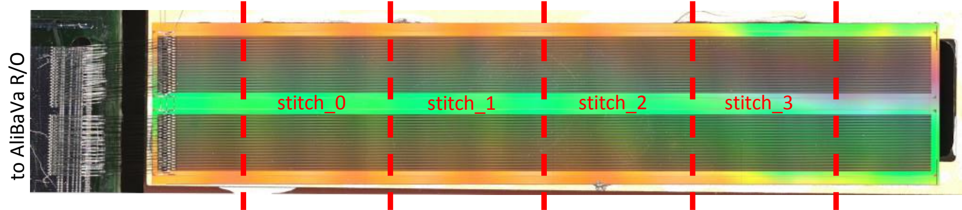
DETECTION EFFICIENCY MEASUREMENT: PIXEL

- R/O chip parameters:
  - Linear FE of RD53A
  - Threshold: 1200 e
  - Noise occupancy: < 10^{-6}
- Efficiency of above requirement (97%)
  - DC and AC, 50 x 50 μm^2 pixels measured
  - Unirradiated at 80 V (V_{dep} + 50 V): 99.85 % efficiency
  - For V > V_{dep}: No difference between AC and DC

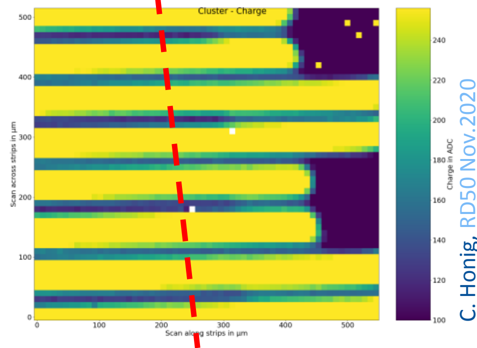


CHARGE MEASUREMENTS: STRIP SENSORS

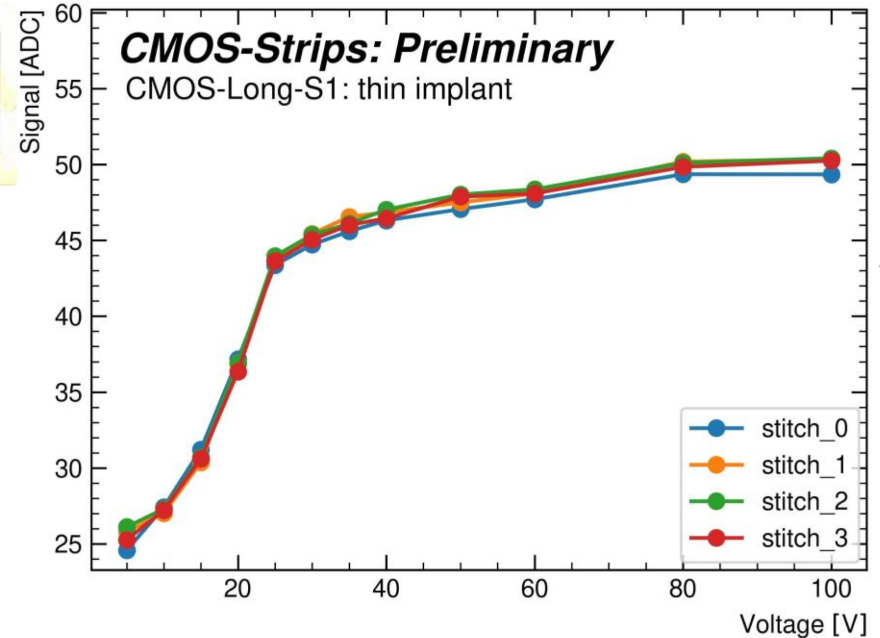
- Strip length > 4 cm ➔ Readout implants across 5 stitches (6 segments)



Laser across two segments



Sr-90 source illuminating different segments

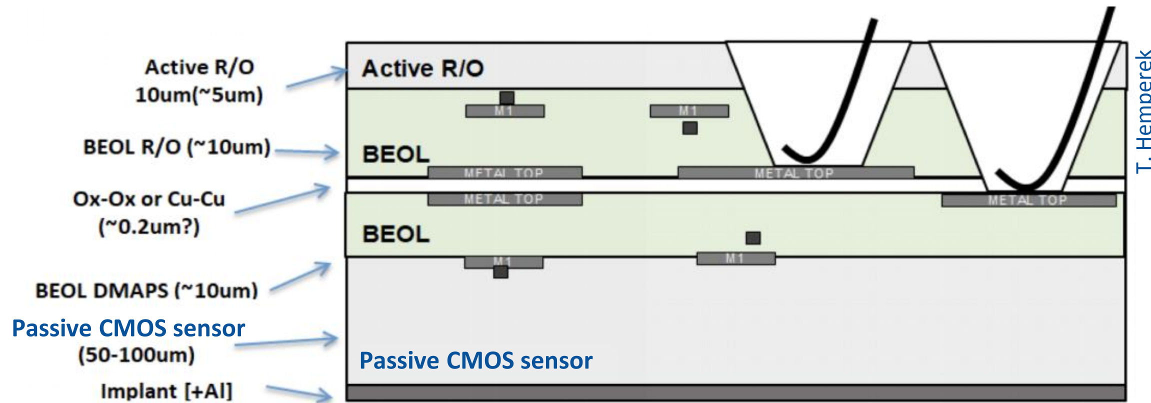


A. Rodriguez, Trento 2021

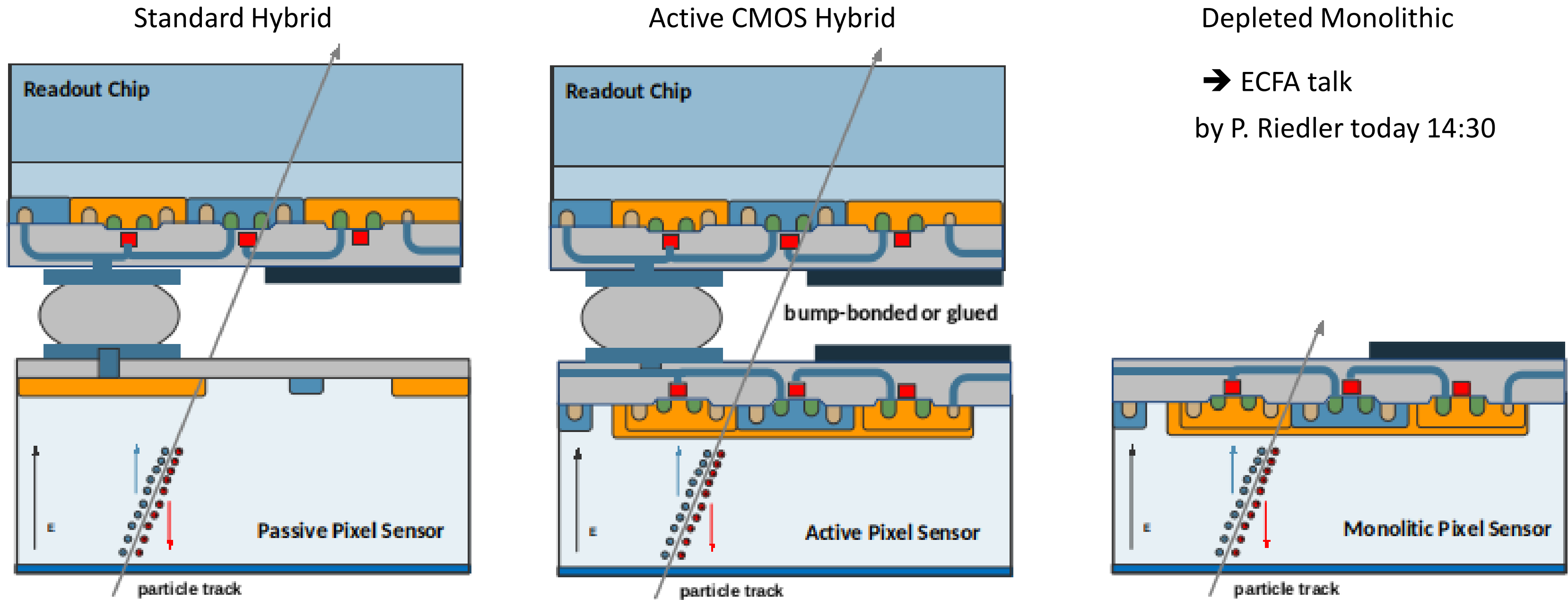
- Charge in all stitched segments the same
  ➔ No negative effect from stitching observed

OUTLOOK: ULTRA-THIN, LOW-COST HYBRID PIXELS?

- Future of hybrid detectors also depends on interconnection technologies:
  - Remove costly and complex chip-to-chip bump bonding ➔ chip-to-wafer / wafer-to-wafer
  - See ECFA Interconnection Technologies talk by T. Fritzsch today 15:00
- Move to wafer-to-wafer bonding (requires compatible FE and sensor wafers)
  - Enables smaller pixel pitches (restricted by bump bonding to ~ 20 um)
  - Thinning after bonding (e.g. sensor 50-100 um; FE ~ 20 um)
  - Requires access to R/O pads from back side (via-last TSV / etching to metal layer on R/O chip)
- Explored within AIDAinnova WP6



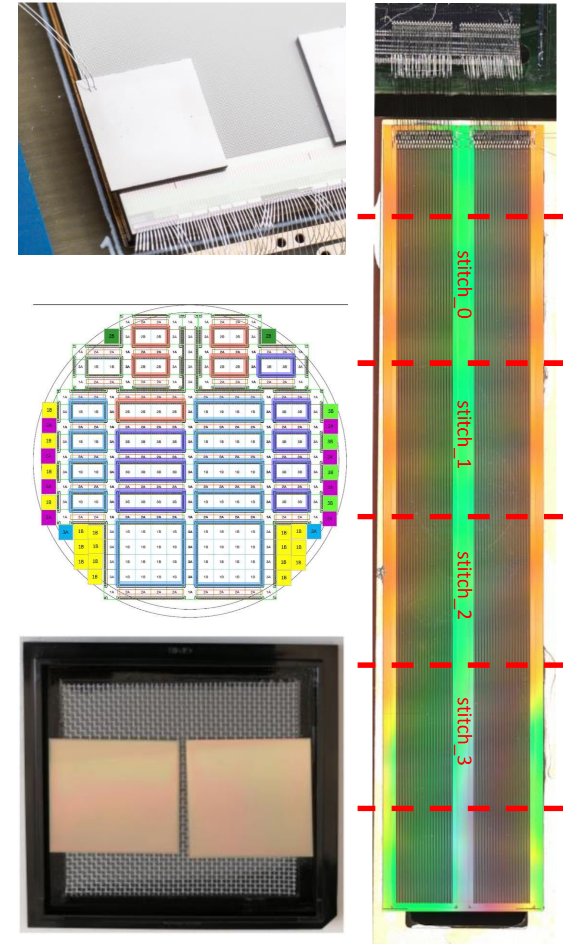
OUTLOOK: ACTIVE CMOS HYBRIDS?



- CMOS active hybrids for high performance solutions (extreme irradiation and hit rates):
  - Active CMOS sensor (amplification included)
  - Digital readout: smaller feature size process for digital logic

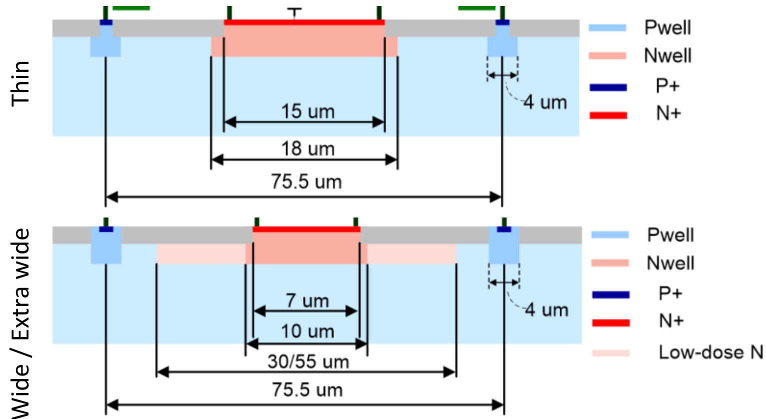
SUMMARY

- Passive sensors using a CMOS process:
  - Access to more vendors for large-scale silicon sensor production
  - Benefits from CMOS process (fast/cheap/process features)
  - Relatively simple designs, easy to port
- Status:
  - Performance is equally good as for „common“ planar sensors (rad. tolerance, detection efficiency, CCE, depletion depth, ...)
  - Stitching for large sensor tiles successfully demonstrated
- The future of „passive CMOS“ depends whether there is a future for passive sensors
  - Large-area hybrid detectors? ➔ R&D for cheaper + easier sensor to R/O interconnections
  - Monolithic sensors could be the more attractive alternative in some scenarios



CAPACITANCE MEASUREMENTS: STRIP SENSORS

- Different geometries of readout implantation

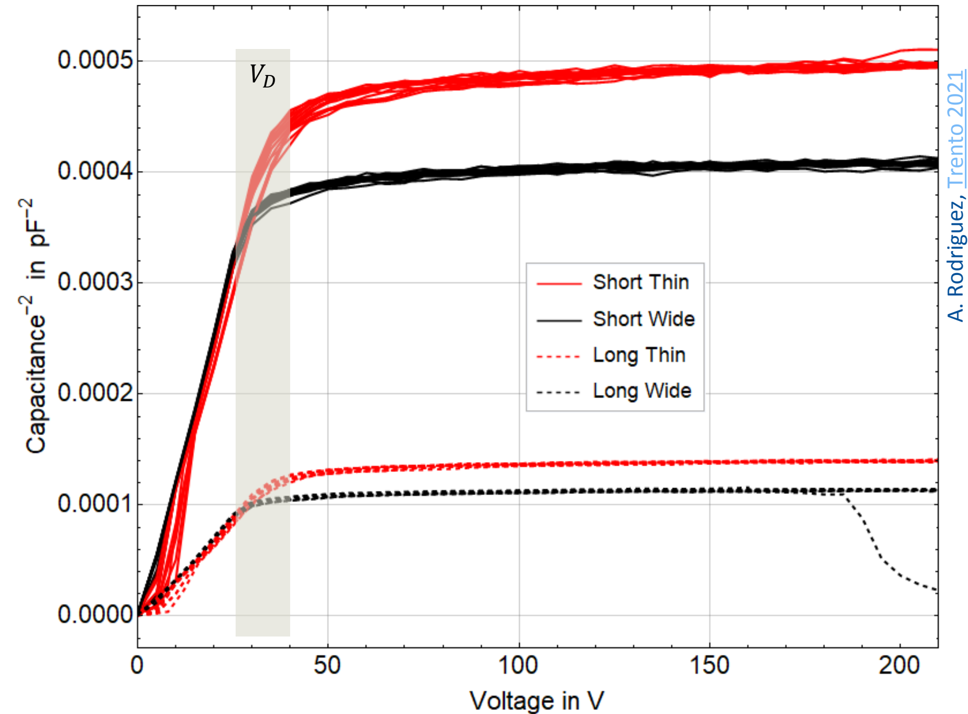


- Capacitance at full depletion ($V_D \sim 25 - 40V$)

Flavor	C / L [fF / mm]
Thin	~ 37
Wide	~ 62
Extra wide	~ 144

preliminary

Capacitance measurement



BACKSIDE PROCESSING

- Changed backside processing vendor to simplify potential production for ATLAS
- First-batch: high current at full depletion V_{dep} ~ 30V, due to inadequate interface from bulk to backside metal
- Increase of implant dose solved issue