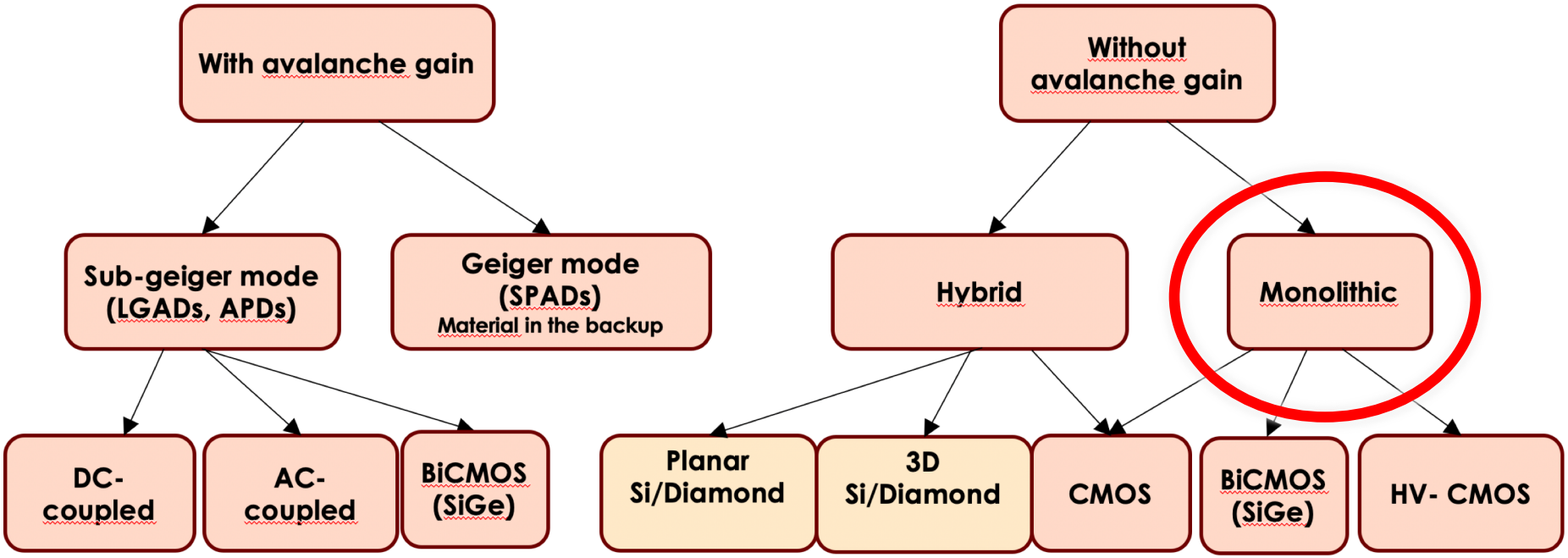
CMOS trackers – present and future developments

Petra Riedler, CERN

Solid state detectors for future (4D) trackers



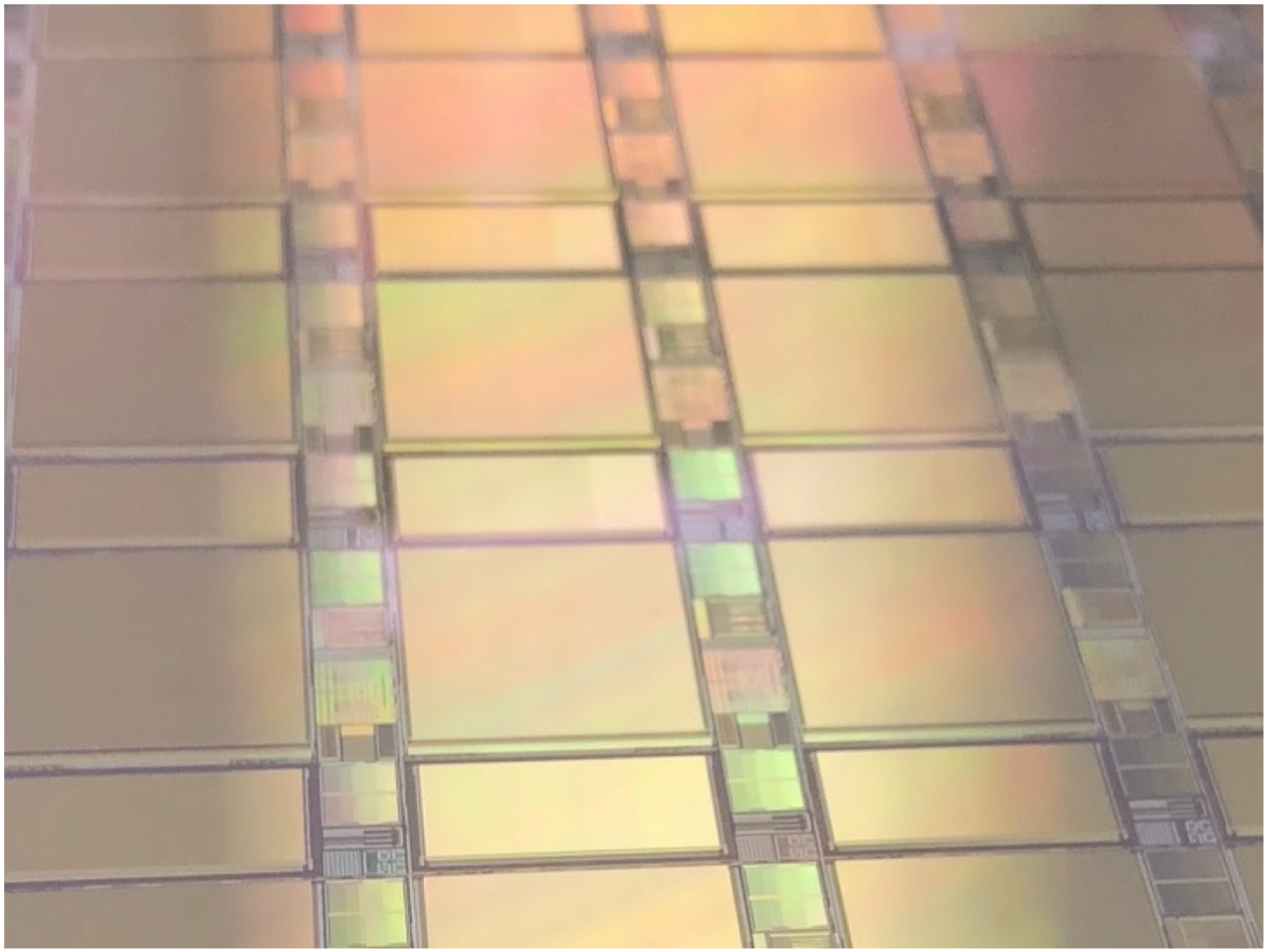
Outlook

- Introduction
- CMOS trackers today
- Developments for future systems and enabling technologies
- Summary

Many thanks to all who have kindly provided material for this presentation:

Jerome Baudot, Manuel Da Rocha Rolo, Forian Dachs, Dominik Dannheim, Nicolo Cartiglia, Magnus Mager, Antonello Di Mauro, Heinz Pernegger, Mateus Vincente Barreto Pinto, Andre Schöning, Abhishek Sharma, Walter Snoeys, Norbert Wermes

Introduction



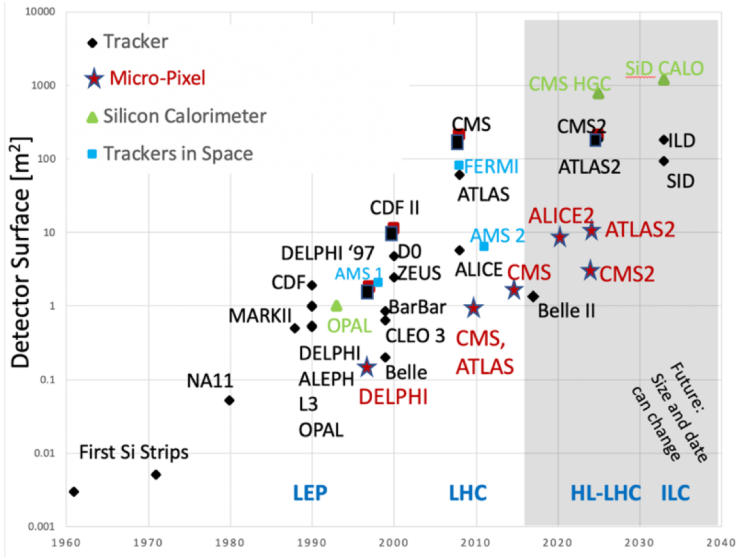
STREAM1 wafer

Silicon trackers get bigger …

For HL-LHC the global surface stays around similar values, but pixel areas increase significantly

ATLAS pixel: 2 m^2 →12 m^2

CMS pixel: 2 m^2 →6 m^2



From F. Hartmann, HST2017

…environments become more challenging

	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	**10^{15}**	**10^{16}**	**10^{15}-10^{17}**
TID	**80 Mrad**	**2x500Mrad**	**>1Grad**
Hit rate [MHz/cm^2]	**100-200**	**2000**	**200-20000**

…number of components increase

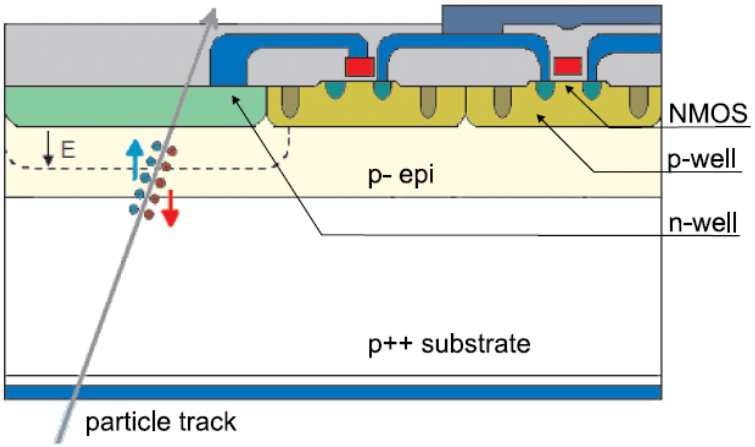
…production, testing and assembly are distributed

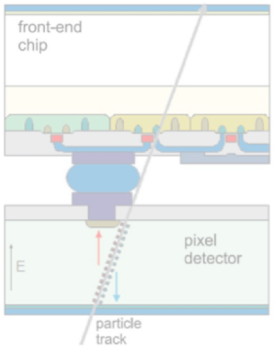
How to build
- **compact,**
- **cost efficient,**
- **reliable and**
- **highly performant**

CMOS sensor modules for the next generation trackers?

CMOS monolithic silicon pixel sensors

Offer a number of interesting aspects that can help to address these points:





Hybrid silicon pixel detector

FE electronics and sensor are integrated in one piece of silicon and produced in commercial CMOS processes → see *talk by W. Snoeys.*

Commercial processes offer high volume and large wafers (200mm, 300 mm) that reduce detector cost and opens possibility for large quantity productions.

CMOS sensors can be thinned to achieve ultimate low mass trackers (0.3% X_0 in Heavy-Ion experiments or <1% for pp).

Small pixel sizes (~20 µm).

No cost (and complexity) of bump-bonding.

Highly integrated modules using industrial post-processing tools.

CMOS sensors – R&D and production

CMOS trackers in HEP have gained enormous momentum over the last years, including the construction of large trackers for LHC such as the ALICE ITS2.

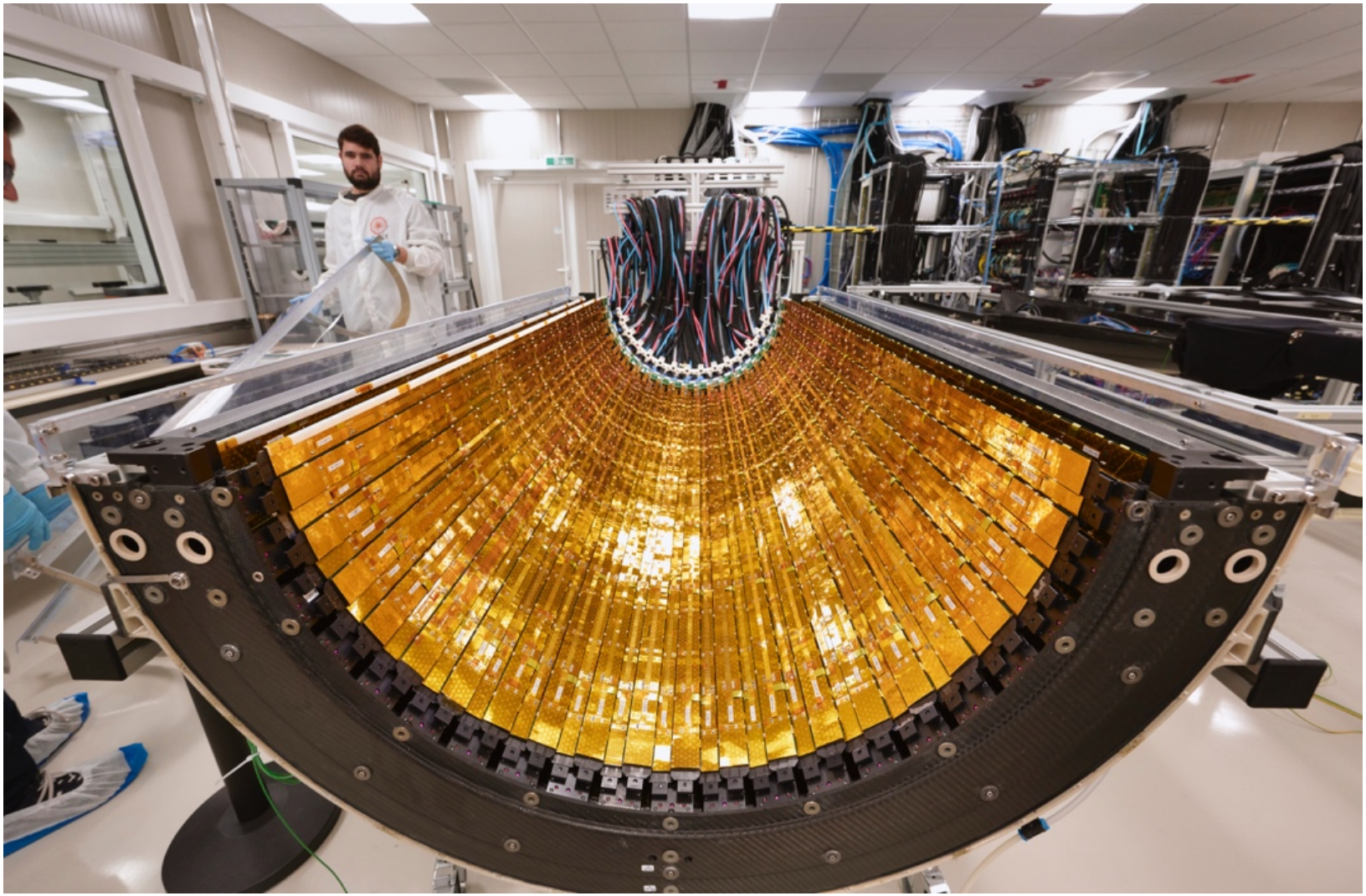
Prior and in parallel there is an **intense R&D activity to study CMOS sensors** for the future, e.g. AIDA2020, STREAM, EP R&D, ARCADIA or AIDAinnova. Not only the **development of the CMOS sensors**, but how to **build modules and systems**.

AIDA 2020 STREAM EP R&D AIDA innova RD50 ARCADIA

Strong activities inside the experiments, such as the ATLAS CMOS collaboration with 25 institutes participating in the development for radiation hard CMOS sensors compatible with the outer layer of the pixel phase II detector.

ATLAS EXPERIMENT

CMOS trackers today

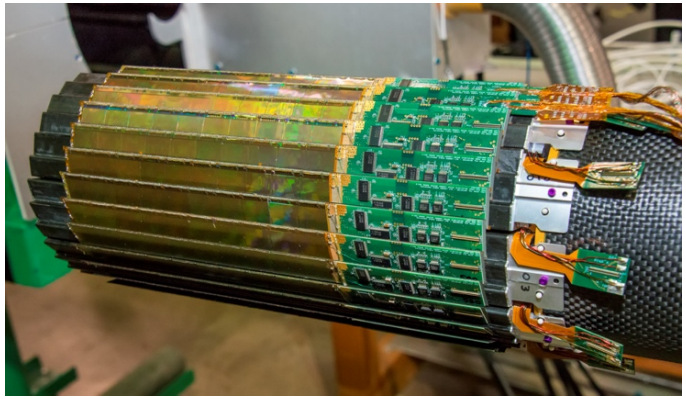


https://home.cern/news/news/experiments/alice-journey-cosmopolitan-detector

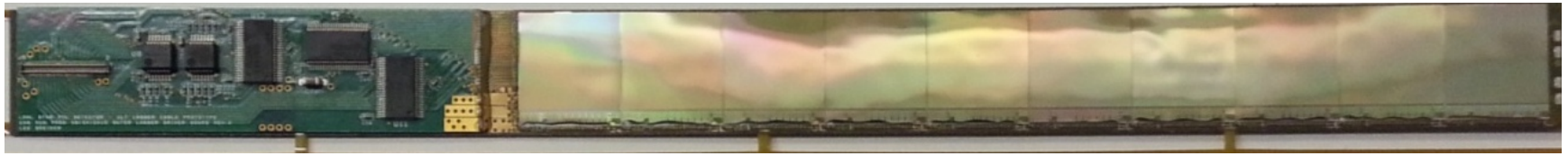
STAR Heavy Flavour Tracker

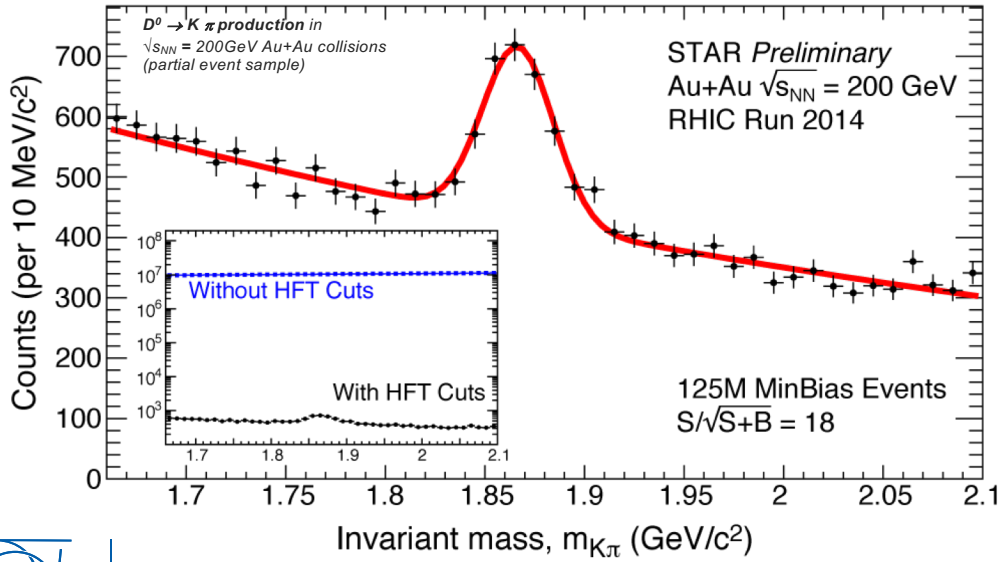
The upgrade of the STAR HFT at RHIC included also the installation of the **first MAPS (MIMOSA-28) based vertex tracker at a collider experiment.**

After R&D and prototyping the construction of 3 trackers started in 2013.



Ladder with 10 MAPS sensors (~ 2×2 cm each)





DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Material budget first layer	X/X_0 = 0.39% (Al cond. cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

ALICE Inner Tracking System – ITS2

Upgrade of the silicon trackers (pixel, drift, strips) for LS2 - Installation currently ongoing!

First CMOS MAPS based tracker at LHC!
Based on high resistivity epi layer MAPS (ALPIDE)

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

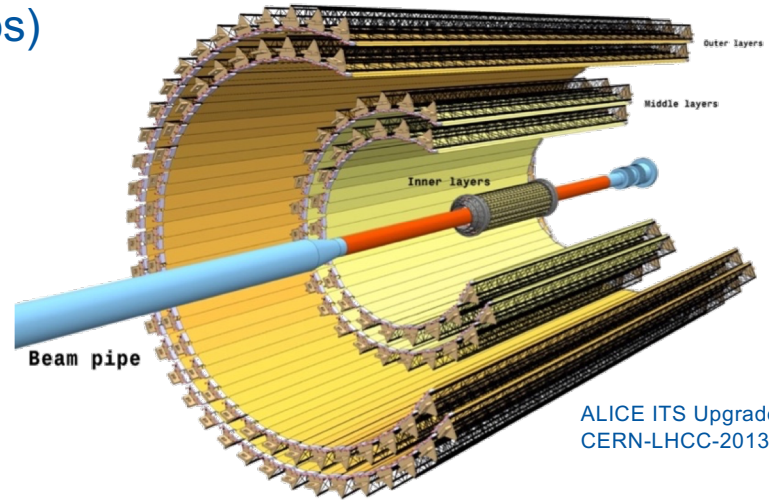
Radial coverage: 21-400 mm

~ 10 m^2, 12.5 Gpixels

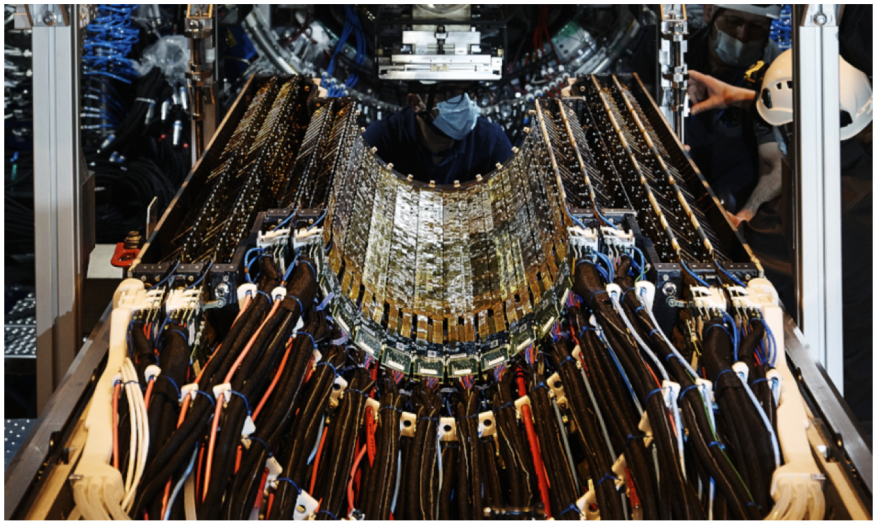
$|\eta|<1.22$ over 90% of the luminous region

0.35% X_0/layer (IB)
1 % X_0/layer (OB)

Radiation level (IB, layer 0): TID: 2.7 Mrad, 1.7 x 10^{13} 1 MeV n_{eq} cm^{-2}



ALICE ITS Upgrade TDR
CERN-LHCC-2013-024



ITS2 outer barrel, picture M. Mager

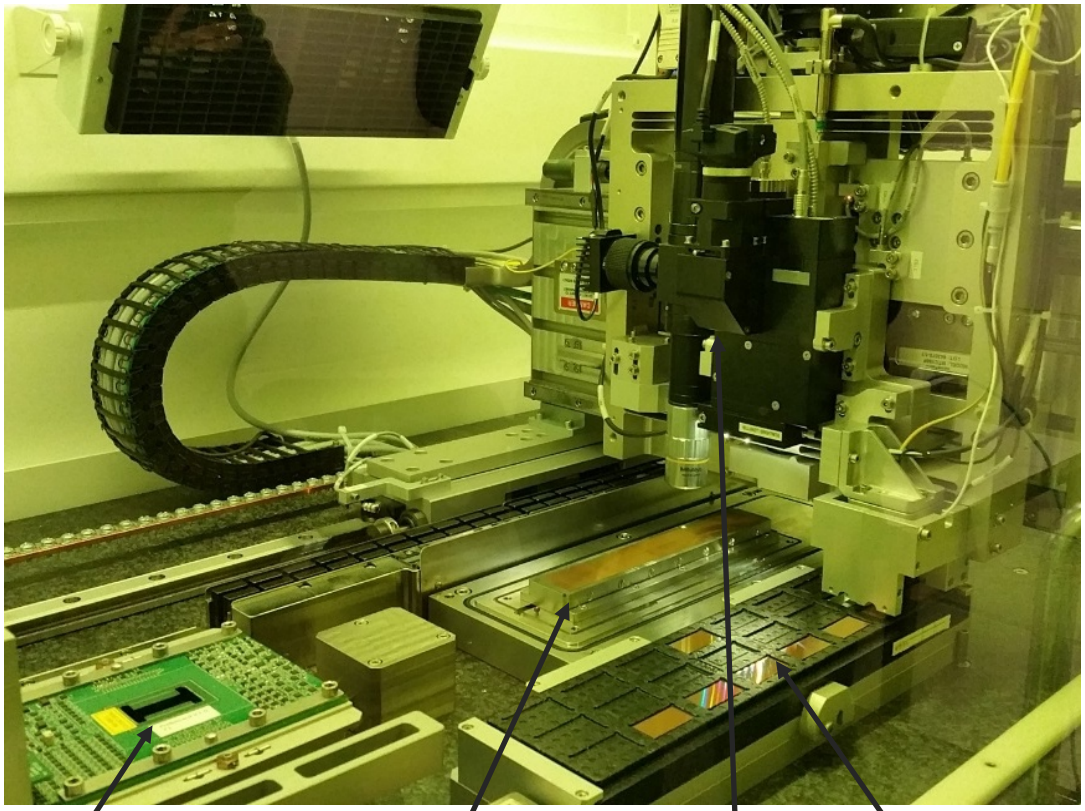
ALICE ITS2 module production

Modules consist of 9 or 14 ALPIDE CMOS chips connected to one flexible printed circuit.

Assembly in a custom machine, which aligns the chips with a position accuracy of +/- 5 µm and provides the possibility to probe the chips and to do a fully automatic visual inspection

→ Customizing and partially automating a large area assembly process

Distributed module construction centers using the same equipment: CERN, Bari, Liverpool, Pusan, Strasbourg, Wuhan.

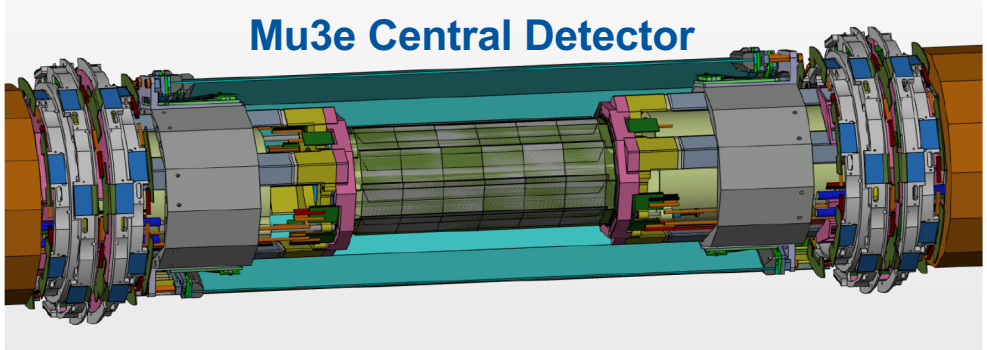


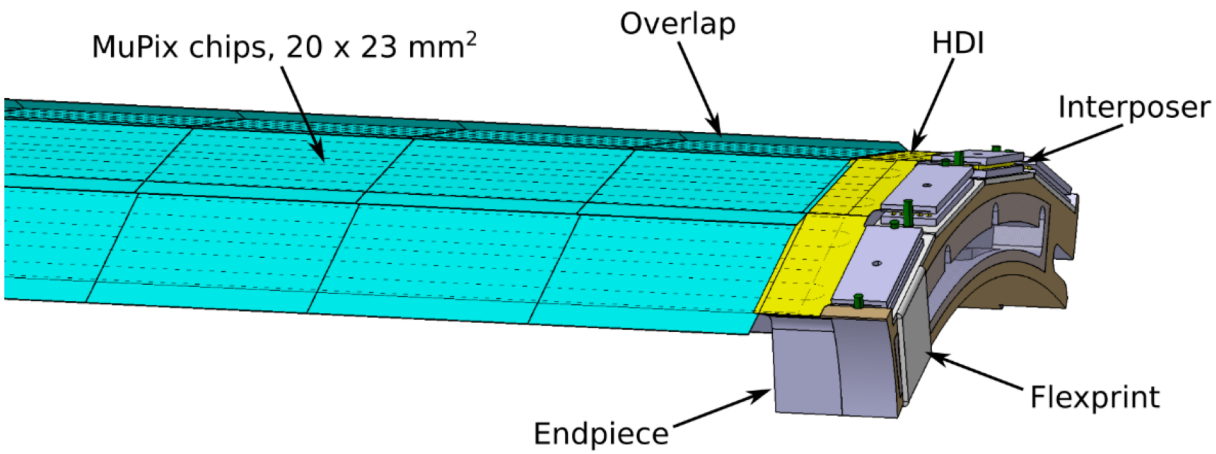
Mu3e

Search for lepton flavor violating decay (PSI) – under construction

HV CMOS based central detector with **ultra-thin HV CMOS pixel sensor modules** (X/X_0= 1.15 per mille)

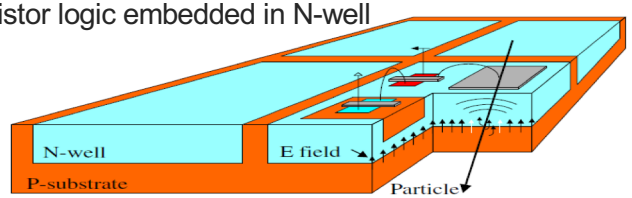
Gas-He cooling system



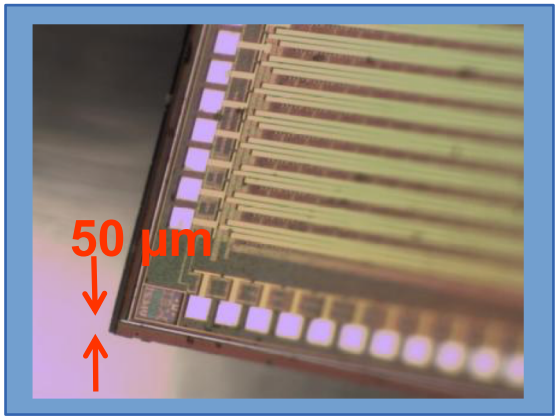


HDI=High density interconnect cable (Al/Kapton)

transistor logic embedded in N-well



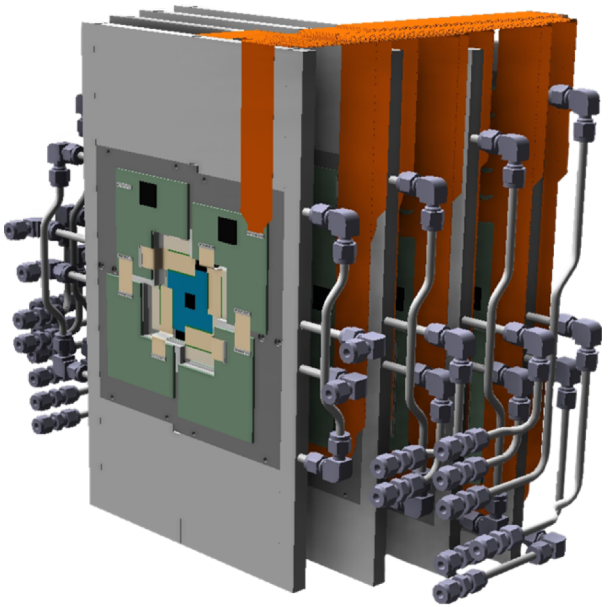
I.Peric et al., NIM A 582 (2007) 876



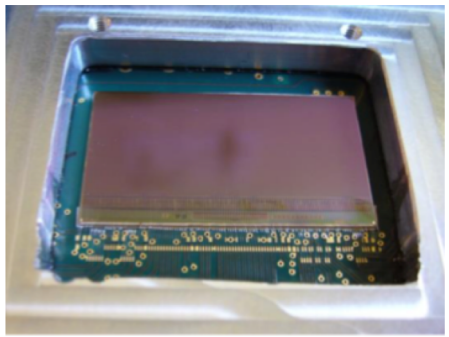
Monolithic pixel sensor in 180 nm HV-CMOS

CBM MVD

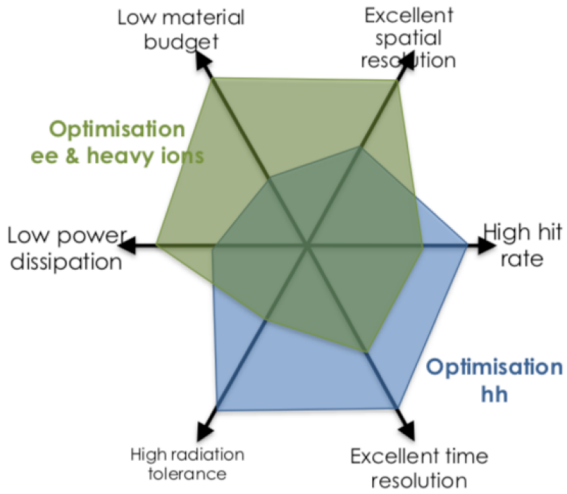
- MicroVertexDetector with **MIMOSIS chips developed in 180 nm TJ process** (following ALICE ALPIDE FEE and priority encoder readout, IPHC-IK Frankfurt-GSI)
- To be operated in vacuum!
- First prototype sensors tested, new submissions with final chip to be submitted in 2023
- **Very light modules**, using double layer concepts.



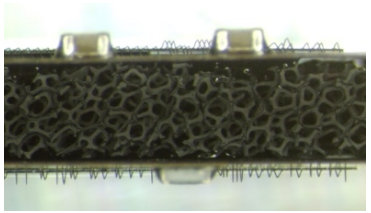
J. Stroth, Bormio 2018



MIMOSIS



	CBM MVD
Spatial res. (µm)	~5
Mat. budget (%X0)	~0,3
Hit rate (MHz/cm²)	15-70
Time figure (ns)	5.10^3
Rad.hard. (kGy) (n_{eq}/cm²)	30 /year < 10^{14} /y.
Sensor	MIMOSIS
Techno (nm)	180 modif.
Pixel pitch (µm²)	27x30
Power (mW/cm²)	< 55



PLUME 2 layer module concept (50 µm MIMOSA26 sensors)

Developments for future systems

Advances in CMOS technologies combined with dedicated designs allowed significant progress in areas like radiation hardness, response time and hit rates.

Strong interest for R&D to fully exploit potential of depleted CMOS sensors in future trackers

- high **granularity**
- low **material budget** and **power**
- **large area** at reduced **cost**
- **Use processes** such as CMOS stitching or RDL to build larger areas
- Build **compact, highly integrated modules**

Adapt technology/design choices on sensor and system level to the needs – overlap but not entirely

Very high particle rates (few GHz/cm^2) and readout rates (>1Gbit/s/cm^2)

Small areas (<m^2) vs large areas (>> m^2)

Very high radiation levels (>10^{15} 1 MeV n_{eq} cm^2)

Low material budget (~1% X_0) vs ultra-low material budget (<0.5% X_0)

Hit timing from ns to µs

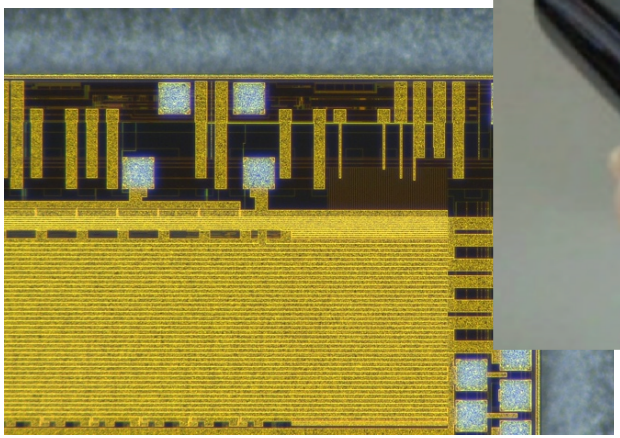
Moderate particle rates (~100MHz/cm^2) and readout rates (<1Gbit/s/cm^2)

Enabling technologies - examples

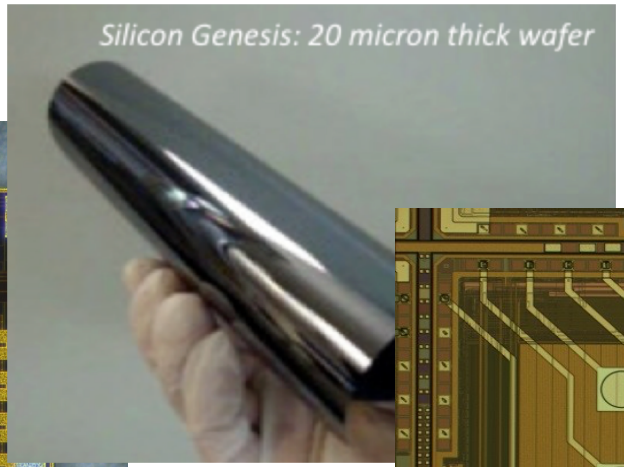
Enabling technologies can be part of the design and foundry fabrication process (e.g. stitching) **and/or include post processing techniques** such as

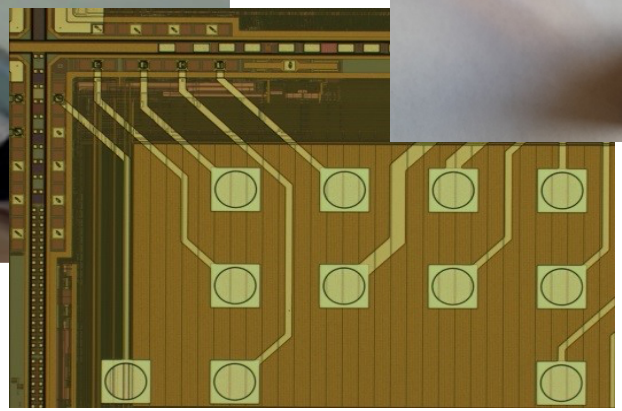
- Thinning and dicing
- Interconnection technologies between sensors and to flex cables
- Wafer level integration technologies

With the aim to build **compact, large area to very large area and highly integrated CMOS modules**.

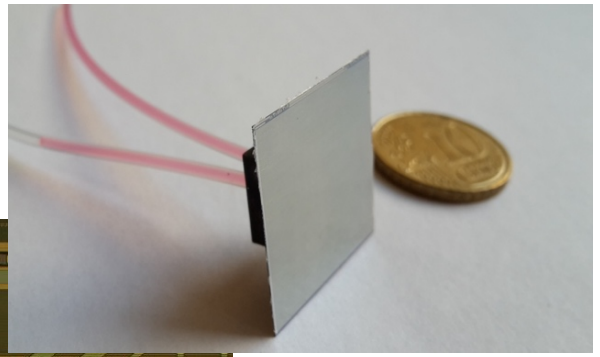


Laser dicing of CMOS sensors (disco.com)





Wafer level RDLs (PacTech.com)



Embedded microchannels in CMOS (EP-DT)

Thinning and dicing

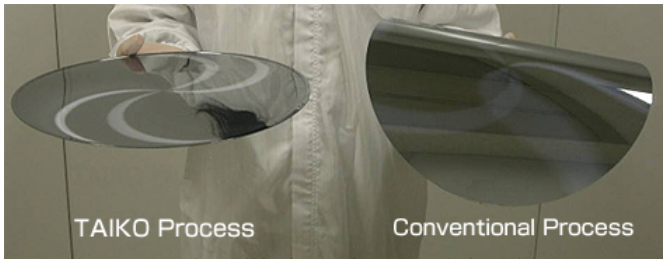
- Many **different dicing techniques** available (blade, laser, plasma,..). Blade dicing is still widely the standard. Some techniques (e.g. plasma) require wafer level processing.

- Challenges for ultra-thin CMOS sensors, to **adapt the process steps** (e.g. opt for DBG-Dice Before Grind). If needed introduce handle wafers to support the thin wafer.

- **Thinning parameters to be optimized**, potentially combined with CMP (Chemical Mechanical Polishing) to achieve back sides with smaller damage and to have better stress control.

→ many options available as industrial service, selecting and optimizing the processes is key to achieve large and thin CMOS sensors

https://www.dicing-grinding.com/services/dicing/

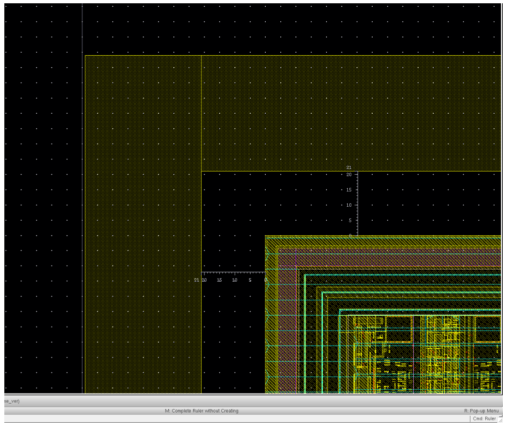


DISCO, 300 mm wafer, 50 microns

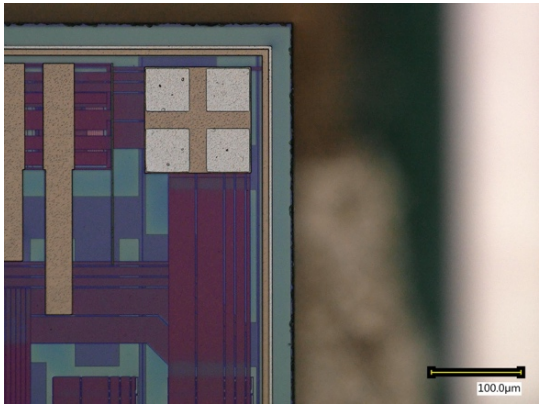
But: also on the design side steps can be taken to improve the dicing and dicing edge quality.

Example: ALPIDE and MALTA

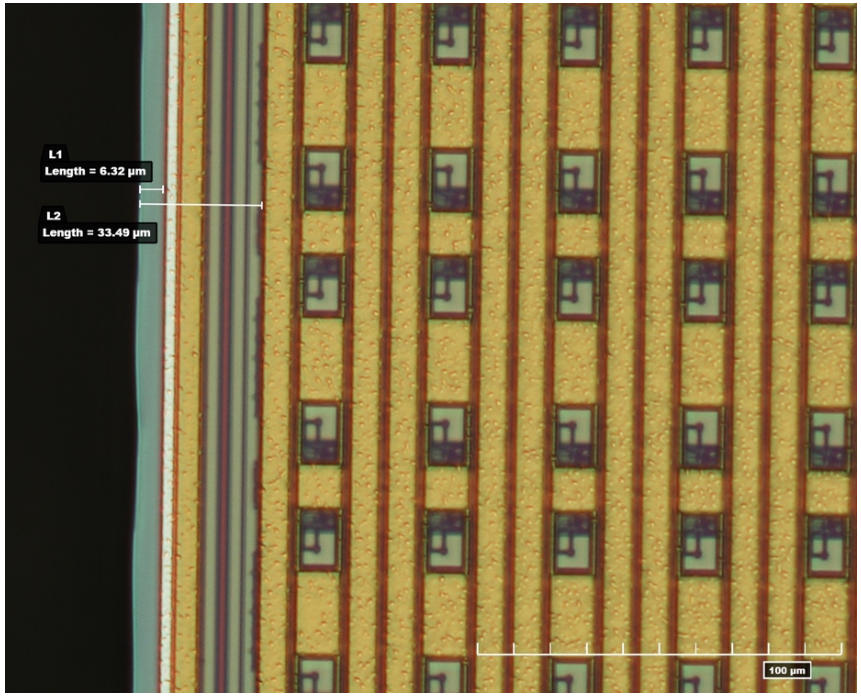
Both chips include a **metal structure free zone of 60 microns around the sealring** to improve the dicing edge quality and for MALTA to allow laser dicing to few microns from the sealring.



ALPIDE corner design



MALTA corner (blade diced)



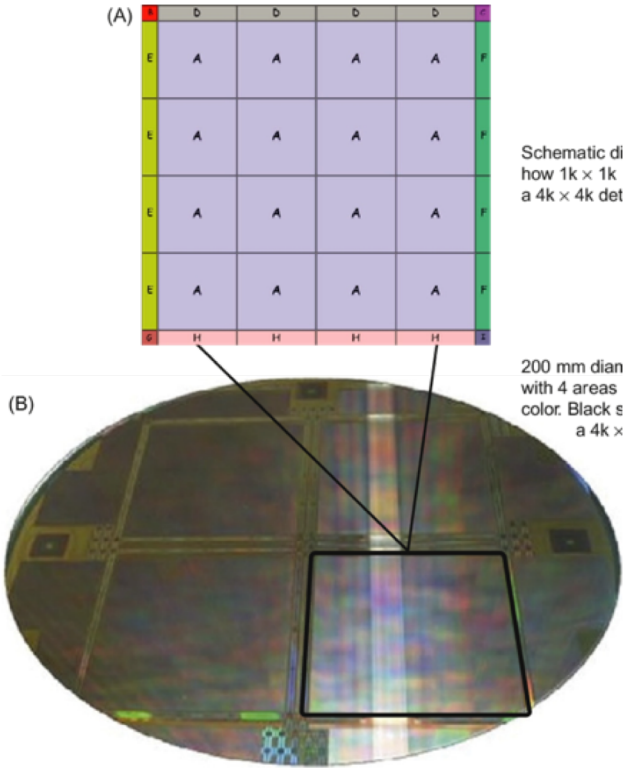
Laser diced MALTA sensor, the cut edge is ~ 6 µm from the sealring. Typical cut distances range from 3-7 µm, thus reducing the inactive edge. Limitation of extending the active area is given by the electronics design.

Large sensors

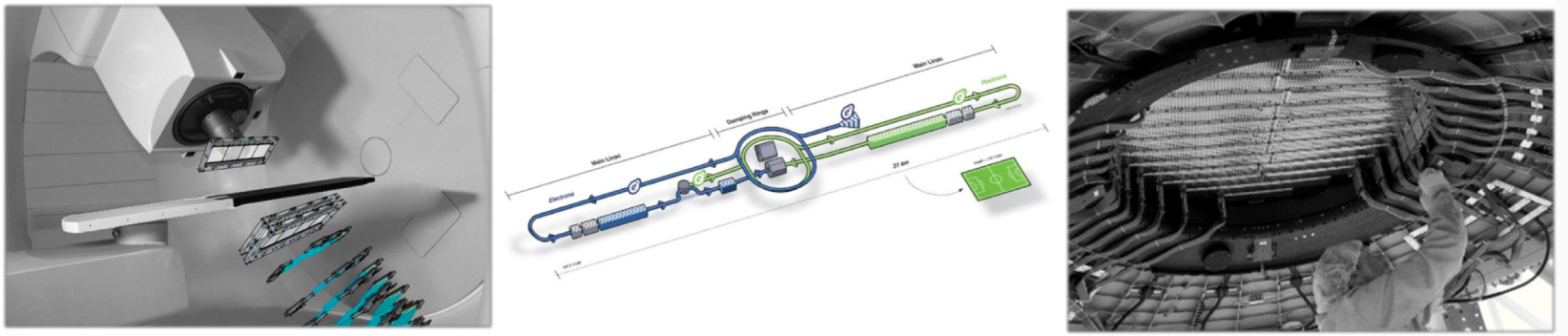
Sensor sizes are usually the size of the reticle (stepping) on the wafer. Typical sizes are ~2 x 3 cm^2.

This limitation can be overcome by **stitching:**

- Sub-blocks of the reticle can be placed in 1D or 2D to achieve a larger sensor. The ultimate limit is the wafer-size.
- Examples of wafer scale sensors have been shown by RAL and are studied within ARCADIA, EP R&D and for the ALICE ITS3 development. Also for passive CMOS sensors (→ *talk by David Leon Pohl*)
- Interesting development not only for HEP, but also for medical and space application (e.g. ARCADIA++).

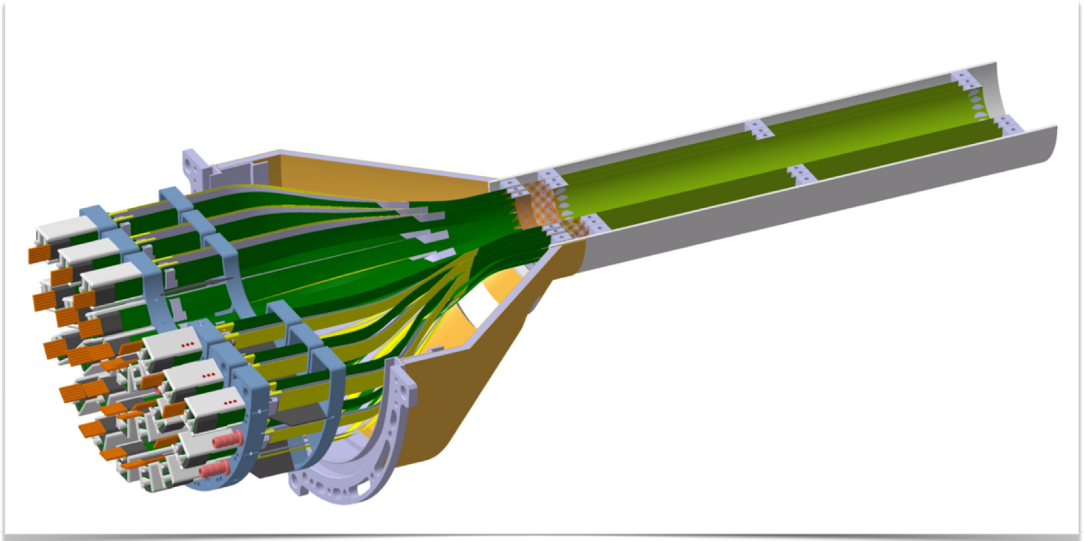


McMullan, G. & Faruqi, A.R. & Henderson, Richard. Doi:10.1016/bs.mie.2016.05.056.



ARCADIA – DMAPS R&D for HEP, medical and space with sensor areas up to 16 cm2 (M. da Rocha Rolo).

ALICE ITS3



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

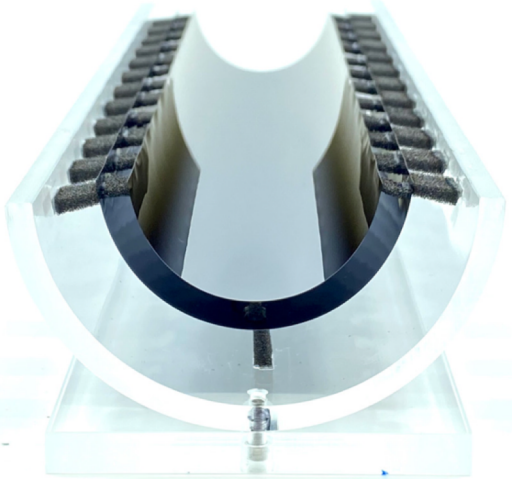
M. Mager, Terascale Workshop 2021

Key ingredients:

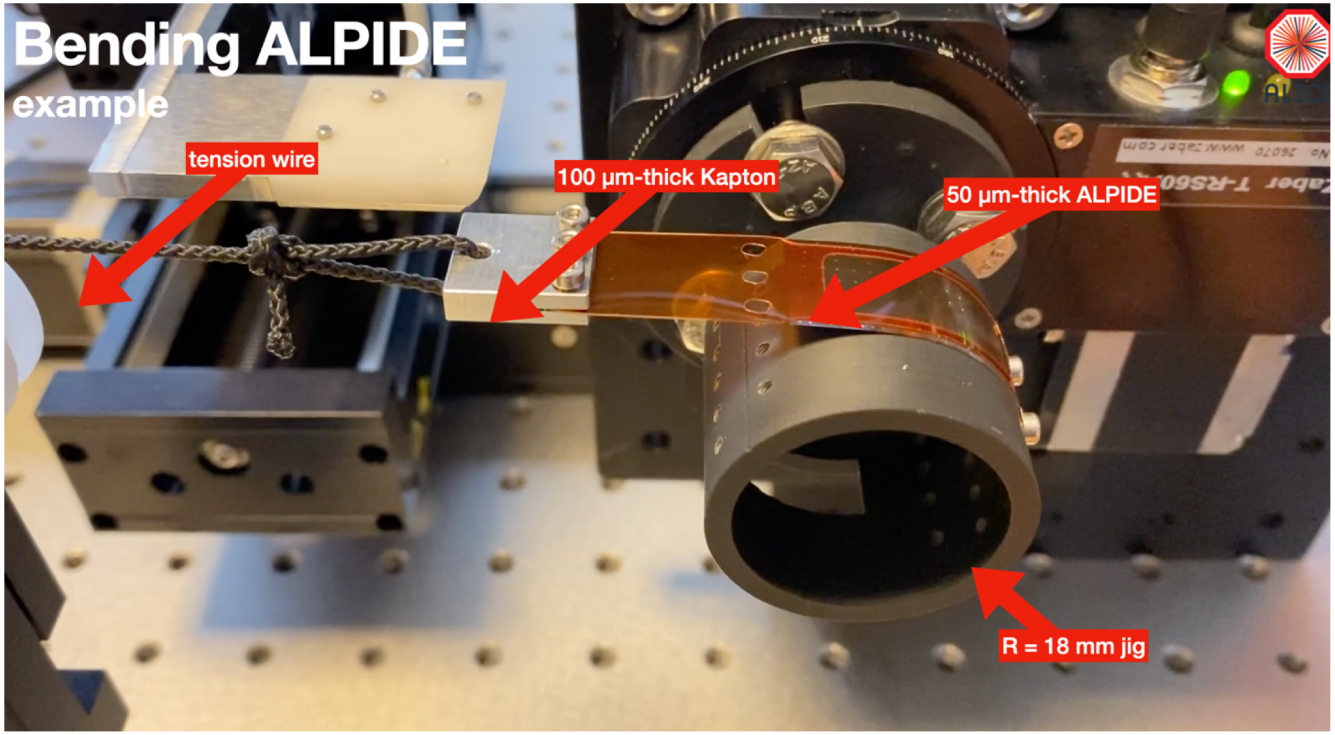
- 300 mm wafer-scale chips, fabricated using stitching
- thinned down to 20-40 µm (0.02-0.04% X0), making them flexible
- bent to the target radii
- mechanically held in place by carbon foam ribs

Key benefits:

- extremely low material budget: 0.02-0.04% X0 (beampipe: 500 µm Be: 0.14% X0)
- homogeneous material distribution: negligible systematic error from material distribution



ALICE ITS3



Tests using 50 micron thin ALPIDE chips:

Different interconnection techniques:

- Wire bonding (before and after bending), spTAB bonding

Testbeam results show perfectly working, with no degradation wrt flat performance.

Next steps:

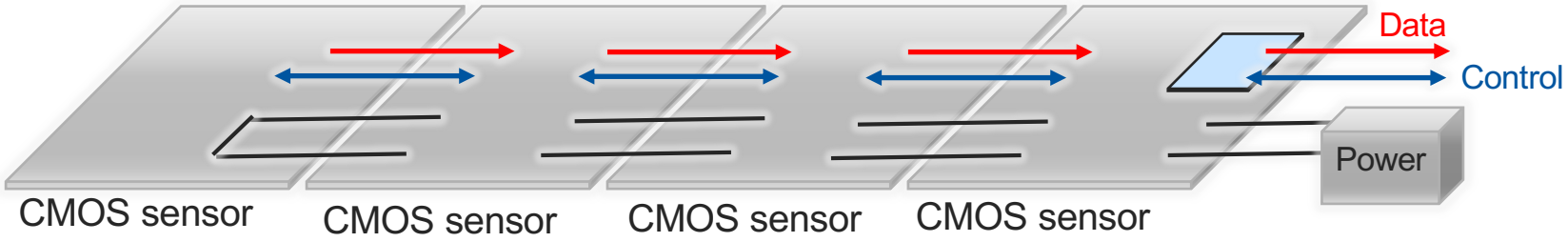
- Dicing blocks of ALPIDE chips (3 x 9) to achieve a 6 cm x 14 cm large “superchip” (still requires individual chip connection)
- Testbeam with 3 bent ALPIDE layers (6 points)
- Test chips in 65 nm process expected end of May →*see talk by W. Snoeys*

M. Mager, Terascale Workshop 2021

Larger system aspects

Consider aspects for integration into larger systems where areas much larger than wafer sizes are needed and/or a modular approach is required, such as:

- Daisy-chain chips (high speed chip to chip connection, power connection)
- Serial powering
- Digital back-end to move time-stamped serialized information and integrating specific requirements (e.g. track trigger, time measurement, etc.)



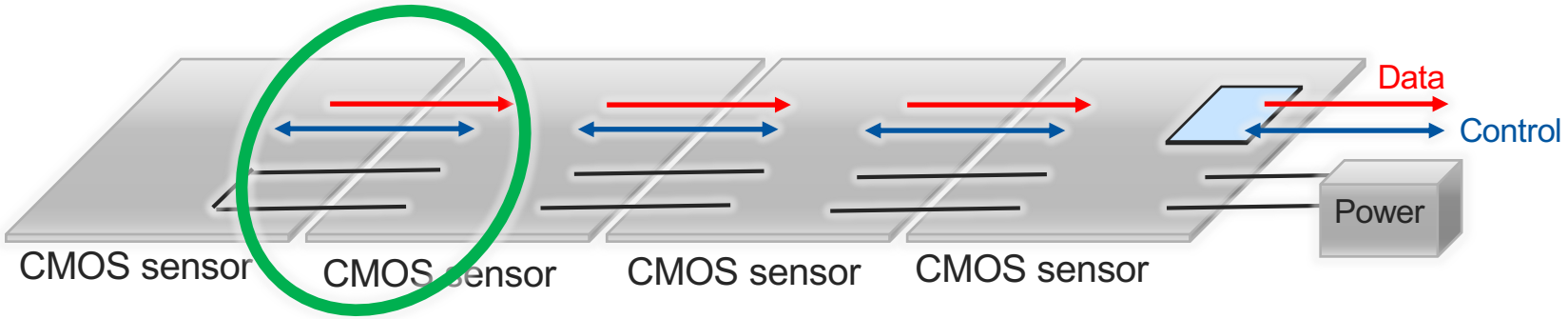
- modular approach, compatible with data volumes
- compact layout with high level of integration into the sensors
- minimizing connectivity using chip-to-chip transfer
- reduce material budget
- optimized assembly process

Interconnection

- Especially, but not only limited to modular concepts, **interconnection technologies to combine data and power from several chips** will allow to achieve larger areas while still maintaining a low material budget (for chip thicknesses of 50 microns and less, the dominant contribution does not come from silicon!)

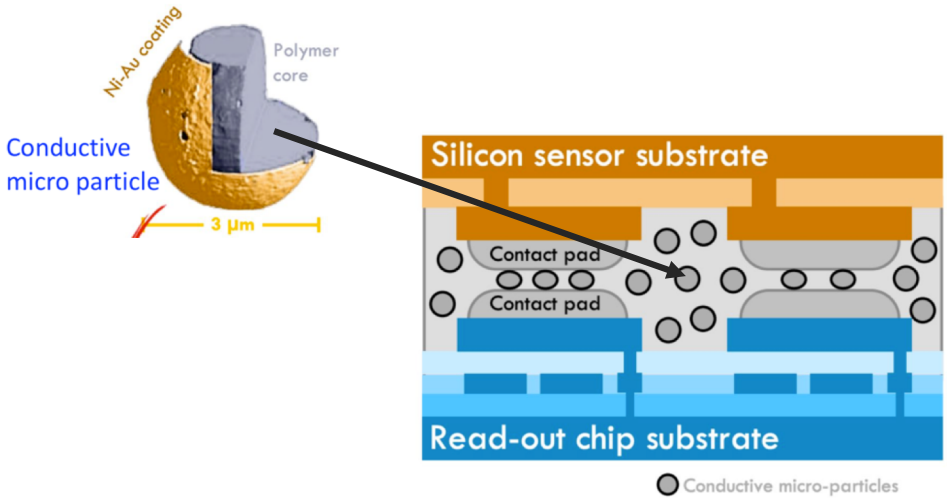
- **Different interconnection techniques** will be interesting to explore – aiming for a reliable, fine granular and radiation resistant connection. An example of a technique under study is ACF (Anisotropic Conductive Film).

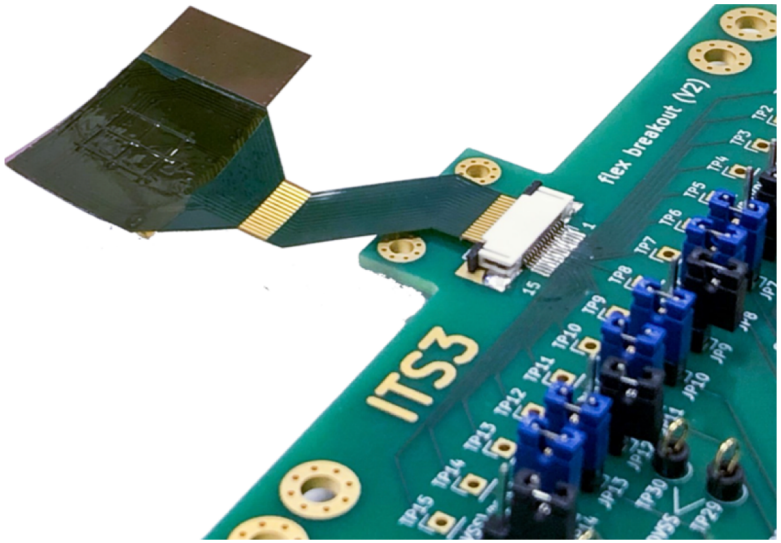
- Exploit special design features for chip to chip data/power transfer.



ACF – Anisotropic Conductive Film

- Studied as alternative to wafer level bump processing but also for module level connectivity.
- It is based on an **epoxy film for mechanical connections, embedded with conductive particles for electrical connections**.
- Prerequisite is mask-less plating of the connection pads (ENIG), which can also be done on a single chip level.
- Can be used in an in-house flip-chip process
- Challenge is the optimization of the ACF film ad the flip chip parameters for small pads.





ALPIDE chip (50 microns) connected to flex-cable.

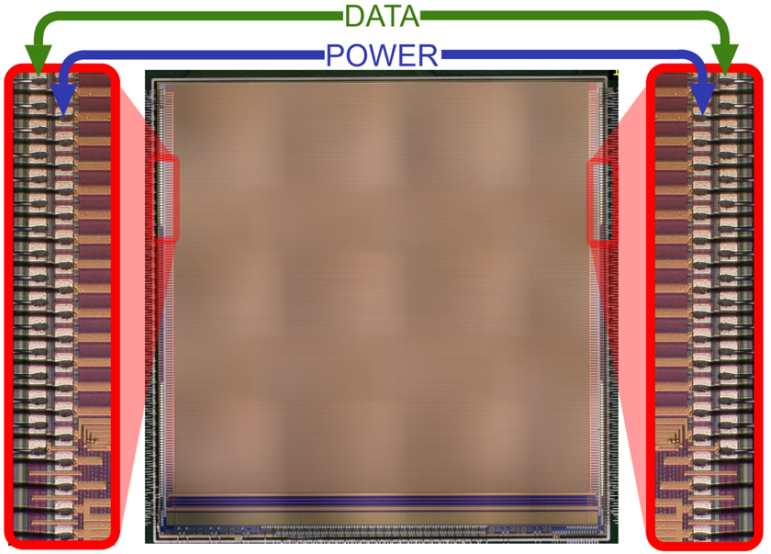
M. Vincente Barreto Pinto

Example: MALTA chip-to-chip communication

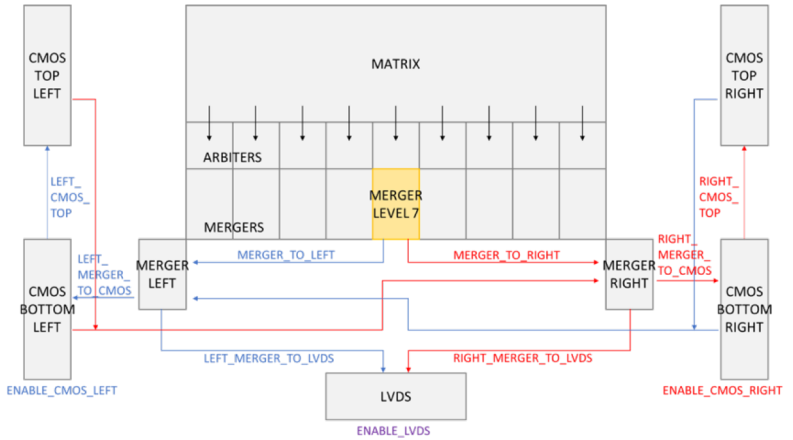
MALTA connection pads: data (CMOS transceivers) can be transmitted between neighbouring sensors.

MALTA includes 40 **CMOS transceivers** on each corner which can be used for **chip-to-chip data transmission** (pulse width 1 ns) as well as **power pads** (analogue and digital) allow to transmit power from one chip to the next.

Data received via these pads can be combined in the chip using the asynchronous internal merger.



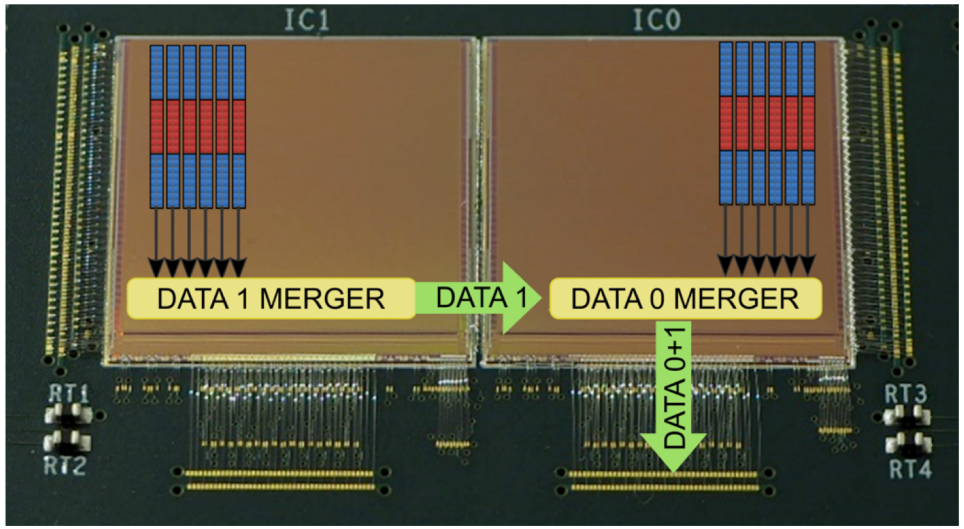
Data and power connection pads on the chip edges. In the MALTA1 version, each chip requires still a separate CTRL and CLK line.

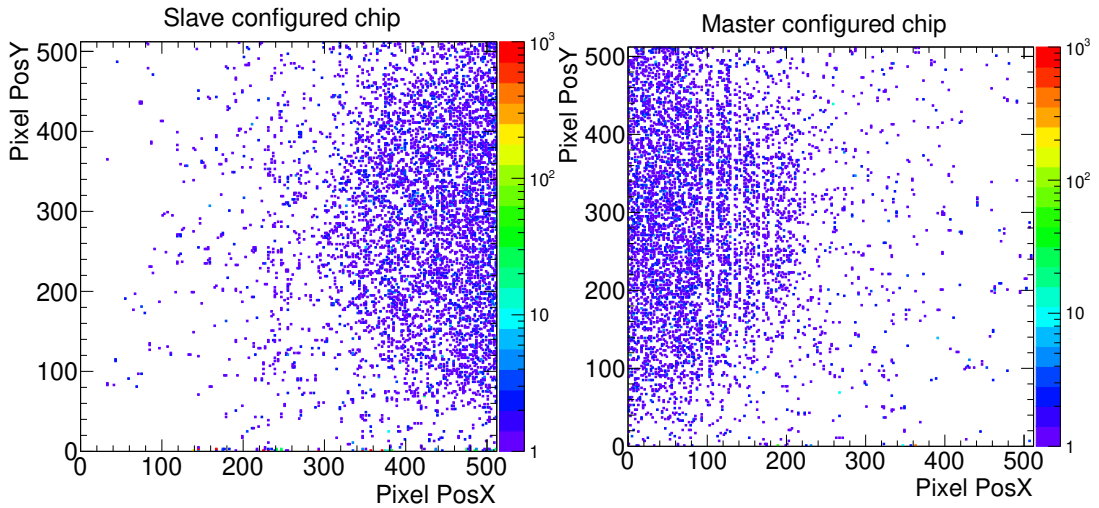


Example: MALTA chip-to-chip communication

- Source tests to validate data transfer from one chip to the other (Sr90 source)
- High speed signal routing from sensor to sensor via edge pads from (GHz)
- All measurements done with same exposure time; white lines are masked double columns

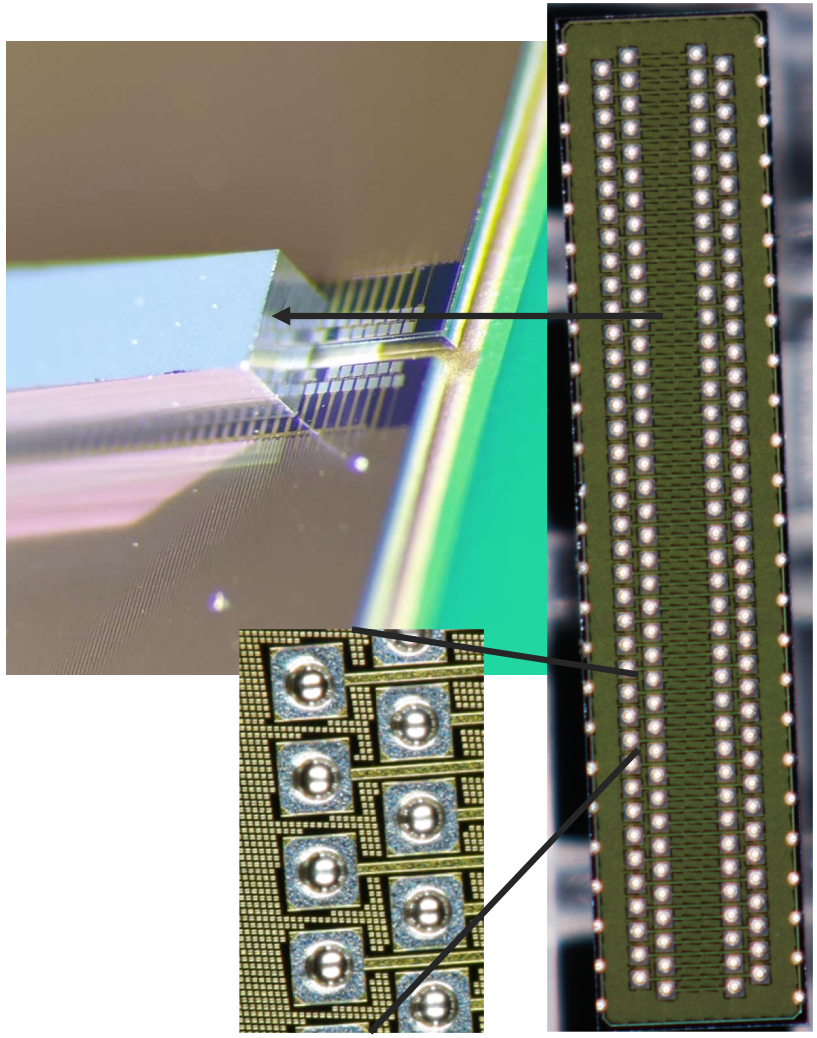
Transfer of data/power from one chip to the next successful, now being extended to 4-chip boards.





Example: MALTA chip-to-chip communication

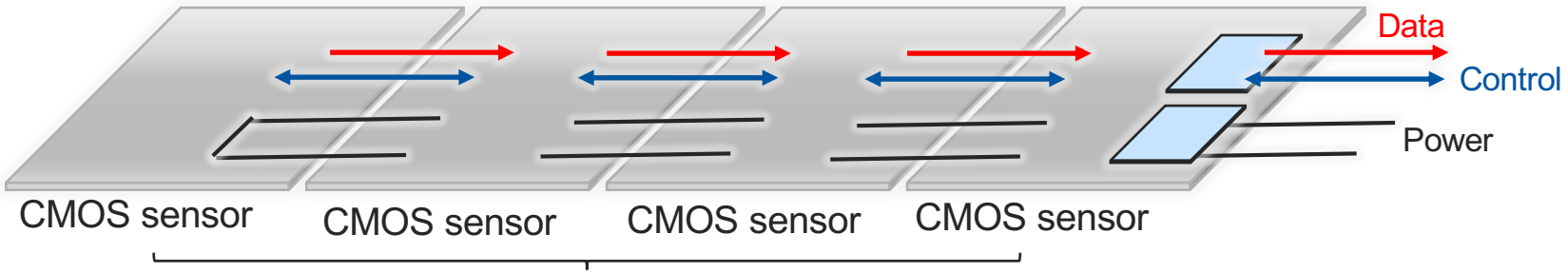
- First (non-functional) MALTA chips with **Si-bridges** using Cu/SnAg studs have been connected successfully. Double chip assemblies are connected also mechanically! (wafer level process)
- In parallel studies using **ACF (Anisotropic Conductive Film)** to connect the Si-bridge with the MALTA sensors are ongoing
- The silicon bridges were produced together with the sensors on the same wafer → could potentially include functionality!
- Pad size (88 µm 88 µm) should be increased to facilitate the connection. Could be done as fan-out using **RDL (Re-Distribution Layer)**



Silicon bridge connecting 2 MALTA chips (F. Dachs)

Larger modules

- Using technologies such as ACF and RDL could allow the **connectivity between chips** (e.g. larger RDL pads to connect two chips with a bridge or flex and ACF), but could also **open the possibility to have modules with simplified connectivity to the outside world.**
  - For example a single/limited point of connection for data transmission could be included at the end of a module (in line with bandwidth limitations) by mounting a transceiver directly on the silicon
  - Potentially a connector for power could be mounted on the silicon for power connections
- This would allow to build very compact modules with the potential to be easily installed/replaced.



or stitched sensor or sensors with wafer level RDL

Summary

- CMOS sensors for trackers have made tremendous progress in the last decade and have been adopted for several projects.
- A very strong and diverse R&D effort is exploring different paths, including novel concepts for trackers.
- Key technologies to build modules will have to include standard industrial processes with the necessary adaptation to HEP experiments.

We have many ingredients to build
- **compact,**
- **cost efficient,**
- **reliable and**
- **highly performant**

CMOS sensor modules for the next generation trackers!