ATCA Developments and Experience at SLAC

VME Replacement Meeting

CERN, 12 July 2012

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Introduction

- SLAC has a much advanced program of generic DAQ components based on ATCA platforms
- SLAC has chosen ATCA as the packaging standard for DAQ components in the work spearheaded by Mike Huffer
- In ATLAS, we have been advocating ATCA-based solutions as an alternative to VME since 2008...
- Many ATLAS-related talks on the topic can be found in Indico by **Mike Huffer, Su Dong, R.B., Martin Kocian and others**
- This talk will recap some of the developments and experience SLAC has had with ATCA
- Applications exist in several running as well as planned experiments – and meanwhile also in ATLAS
- Future applications have been proposed and are under study

Outline

- A brief history of ATCA at SLAC (and ATLAS)
- Why we chose ATCA as packaging standard
- First generation of generic DAQ boards on ATCA: RCE and CI ("Gen-I")
- Cluster-on-board (COB) technology with second generation RCE as mezzanine card ("Gen-II")
- Existing, planned and proposed applications
- Answers to Philippe's questions (as they apply to core DAQ)
- Summary & Conclusions

SLAC has been advocating ATCA for a while...

ATLAS TDAQ upgrade proposal

TDAQ week at CERN

Michael Huffer, mehsys@slac.stanford.edu
November 19, 2008

**Introduction to ATCA & DAQ building blocks.
Any ATLAS applicability ?**

ATLAS upgrade week at CERN

Michael Huffer, mehsys@slac.stanford.edu
February 25, 2009

CERN/ACES Workshop

A new proposal for the construction of high speed, massively parallel, ATCA based Data Acquisition Systems

Michael Huffer, mehsys@slac.stanford.edu
Stanford Linear Accelerator Center
March, 3-4, 2009

> No longer an ~~emerging~~ standard!
> → mature

SLAC Department of Particle Physics & Astrophysics — Office of Science/ U.S. D.O.E.

Why ATCA as a packaging standard?

- An emerging *telecom* standard...
- Its attractive features:
  - backplane & packaging available as a *commercial* solution
  - generous form factor
    - 8U x 1.2" pitch
  - hot swap capability
  - well-defined environmental monitoring & control
  - emphasis on High Availability
  - external power input is low voltage DC
    - allows for rack aggregation of power
- Its **very** attractive features:
  - the concept of a Rear Transition Module (RTM)
    - allows all cabling to be on rear (module removal without interruption of cable plant)
    - allows separation of data interface from the mechanism used to process that data
  - high speed serial backplane
    - protocol agnostic
    - provision for different interconnect topologies

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... and many more presentations, 2-day training workshop, etc.

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History of Generic DAQ R&D at SLAC (I)

- Phase-I
  - » *"Survey the requirements and capture their commonality"*
  - » Intended to **leverage recent industry innovation**
  - » Project had a cultural bias: "one size does not fit all"
  - » Introduction of the concept of ubiquitous building blocks
    - The (Reconfigurable) Cluster Element (RCE)
    - The Cluster Interconnect (CI)
    - **Industry standard packaging (ATCA)**
  - » Technology evaluation & demonstration hardware
  - » The RCE & CI boards
  - » Meet ¼ of identified performance goals

History of Generic DAQ R&D at SLAC (II+III)

- Phase-II
  - » Useful, sustainable architecture (how to future proof)
  - » Generic ATCA Front-Board (the COB)
  - » The RCE "Gen-II"
  - » Meet ½ of all performance goals

  > Currently nearing
  > the end of Phase-II

- Phase-III
  - » Move from PowerPC to ARM processor architecture
  - » Cost & power optimized design
  - » Meet all performance goals

ATCA as a Packaging Standard

- Now an mature telecom standard…
  - » Developed and sanctioned by PICMG (PCI)
  - » More than 10 years old and deployed world-wide
  - » *See Markus' earlier talk*
- Its attractive features:
  - » Slot/card based (2, 5, 14 & 16 slot shelves)
  - » Backplane & packaging available as a commercial solution
  - » (Relatively) generous slot form factor, 8U x 1.2" pitch
  - » Emphasis on high availability, lots of redundancy
  - » Hot swap capability
  - » Well-defined environmental monitoring & control (IPMI)
  - » Pervasive industry use
  - » External power input is low voltage DC
    - · Allows for rack aggregation of power

ATCA as a Packaging Standard (cont.)

- Its *very* attractive features (that influenced our choice as substrate for the RCE & CI components):
  - » The concept of a Rear Transition Module (RTM)
    - Allows all cabling on rear (module removal without interruption of cable plant)
    - Allows separation of data interface from the mechanism used to process that data
  - » High speed serial backplane
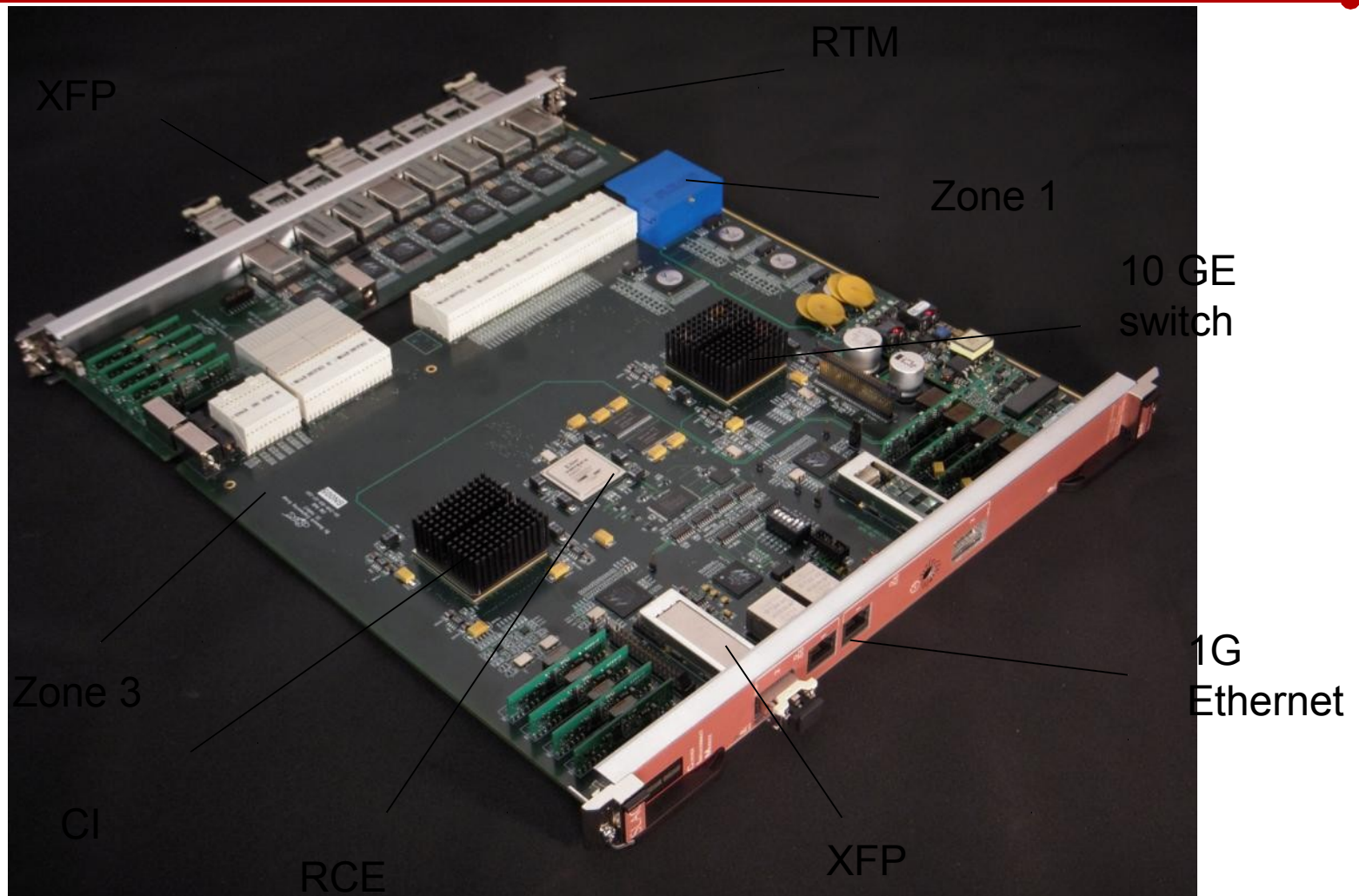   - Protocol agnostic
    - Provision for different interconnect topologies
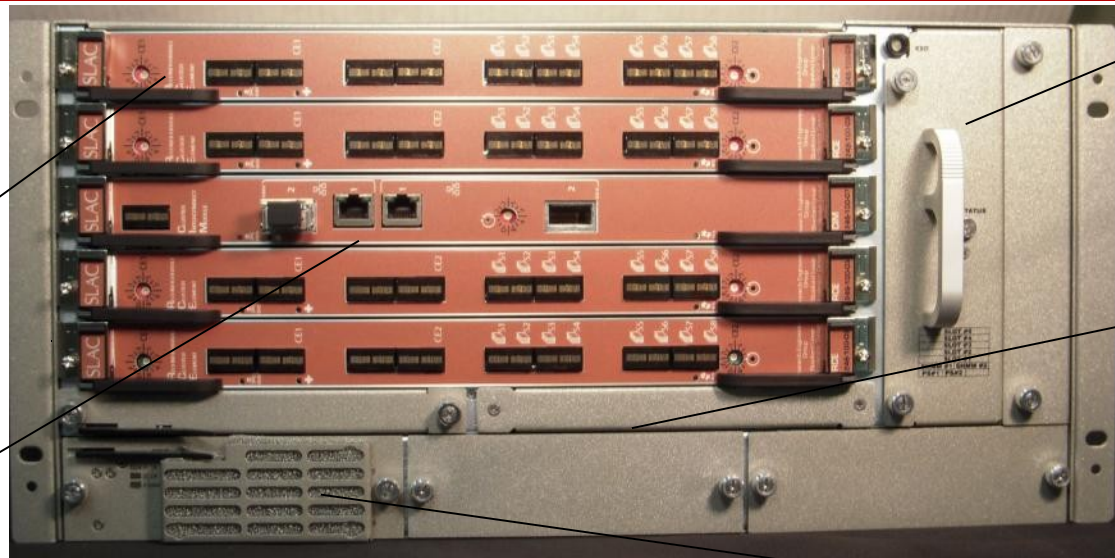
Gen-I RCE Board + RTM

transceivers

RTM

Zone 1 (power)

Zone 2

Zone 3

RCE

Media Slice controller

Media Carrier with flash

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Gen-I CI Board + RTM

XFP

RTM

Zone 1

10 GE switch

Zone 3

CI

RCE

XFP

1G Ethernet

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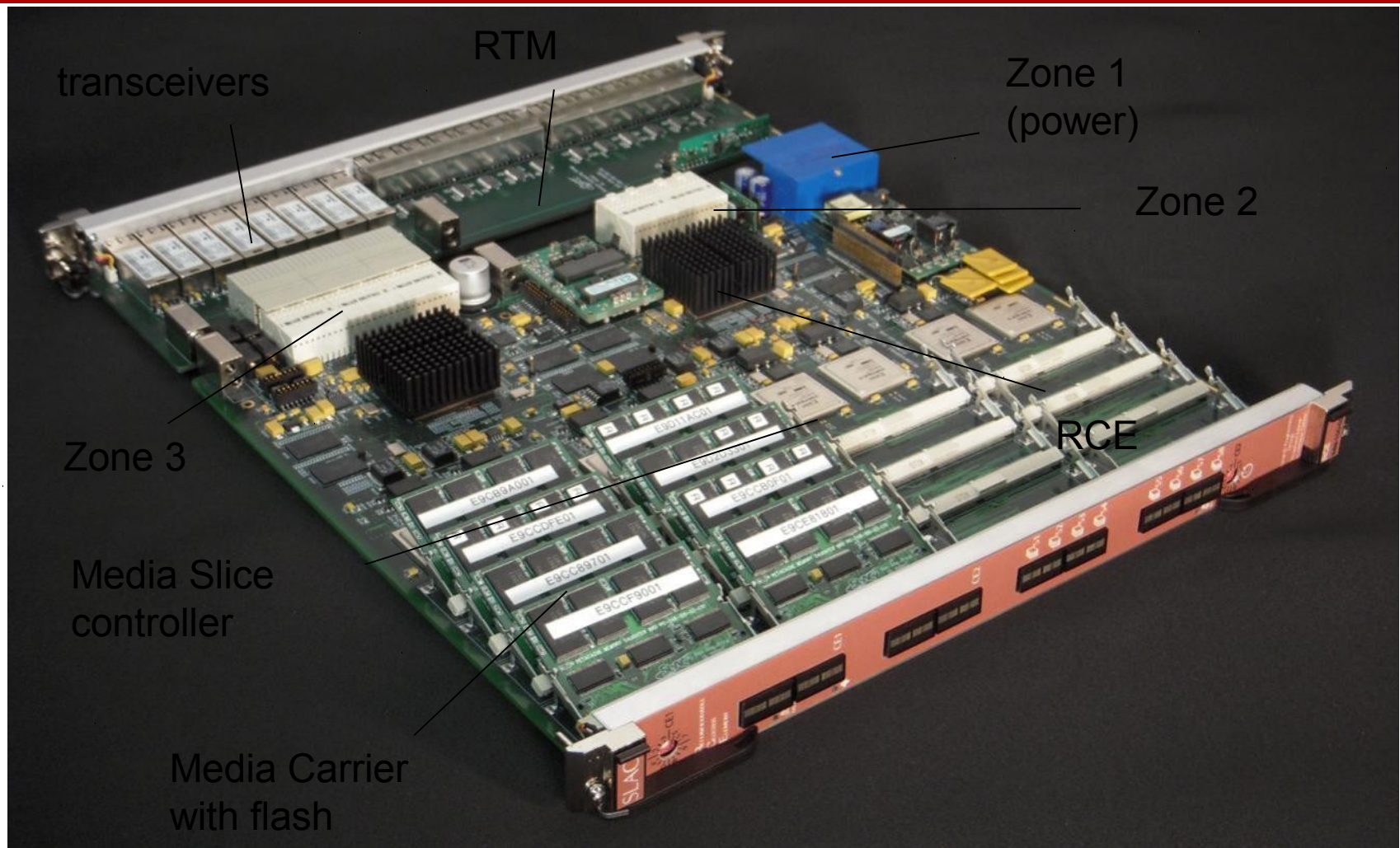
Typical (5 Slot) Shelf

Front

front board

front board

Back

fans

Shelf manager

Power supplies

RTM

RTM

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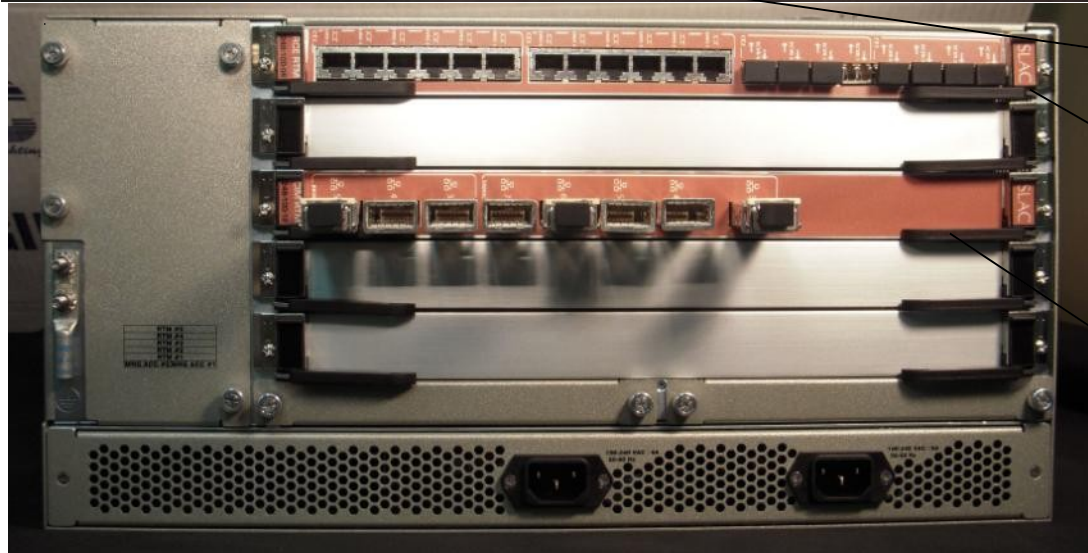
The Cluster On Board (COB)

- "Mezzaninize" RCE & CI concepts
  - » Decouples RCE & CI from ATCA (or any packaging standard)
- New ATCA Front-Board (the COB) which supports:
  - » The mezzanine concept
  - » Decouples front-board from RCE & CI
  - » IPMI (shelf configuration & monitoring)
  - » Targeted towards full-mesh backplanes
  - » Applications require only a single type of board
  - » Interoperability with any type of backplane
  - » The "ATCA RTM for physics" standard (PICMG 3.8)
  - » Complete interoperability with any type of ATCA board
  - » 10 Gbits/s signaling (both backplanes & Ethernet switching)
  - » Generic, synchronous Timing & Trigger signal distribution

The Gen-II RCE Hardware Infrastructure

Resources per RCE:

- Xilinx Virtex 5 FX70 FPGA with built-in crossbar & increased user firmware application space
- 4 GByte memory
- 6 channels of data I/O up to 12.5 Gb/s per channel.
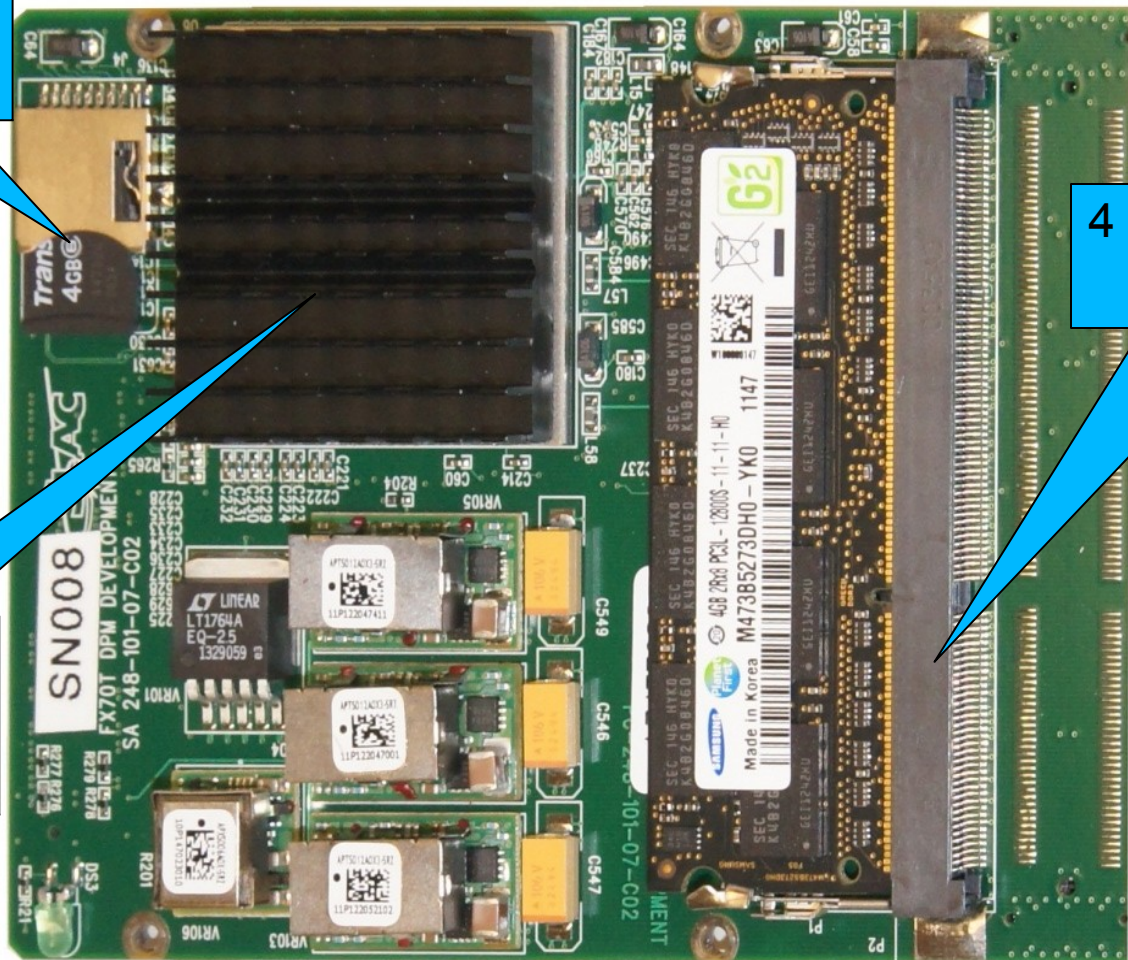- 40 Gb/s Ethernet network output
- 128 DSP tiles
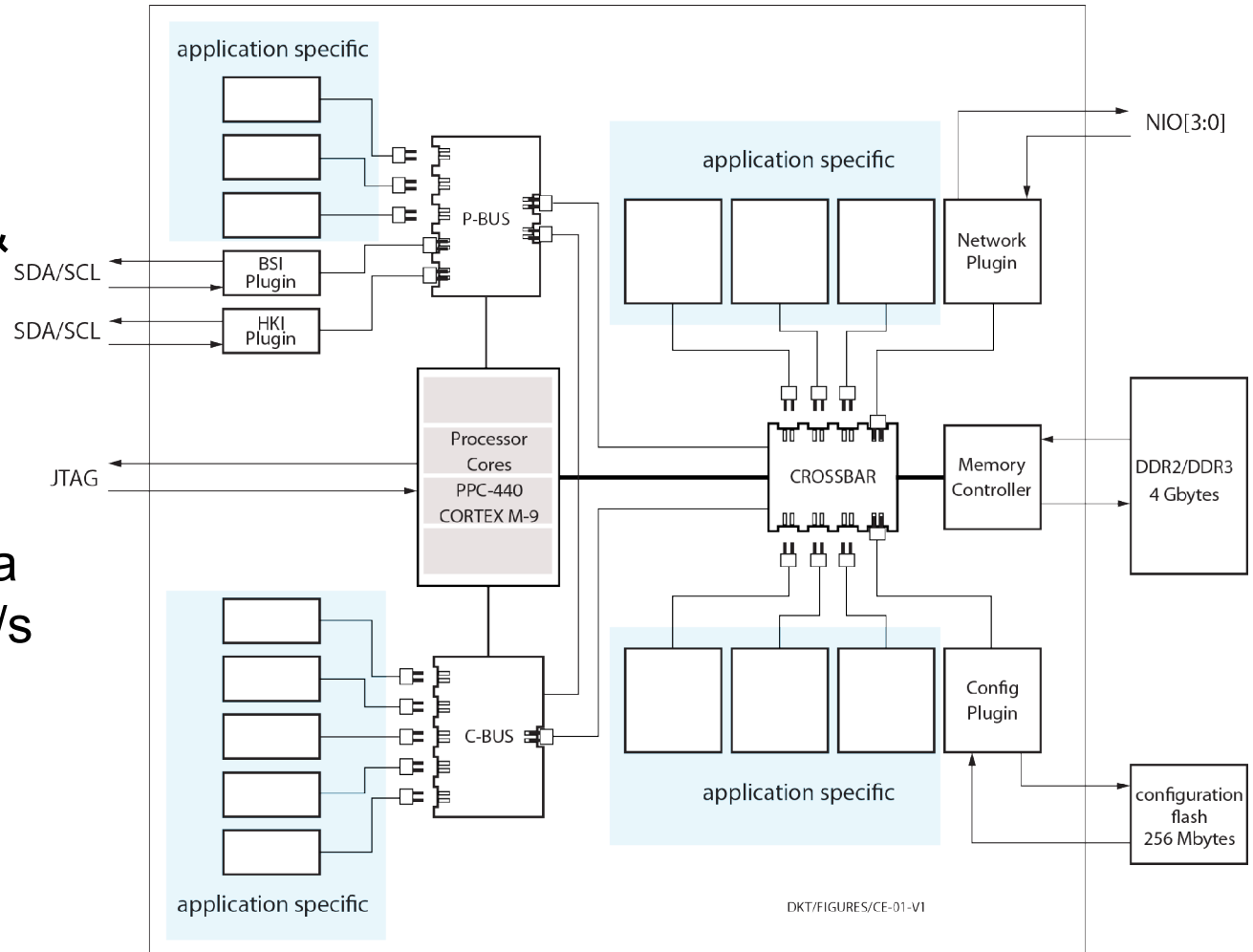
Single-Element (Gen-II) Mezzanine Board
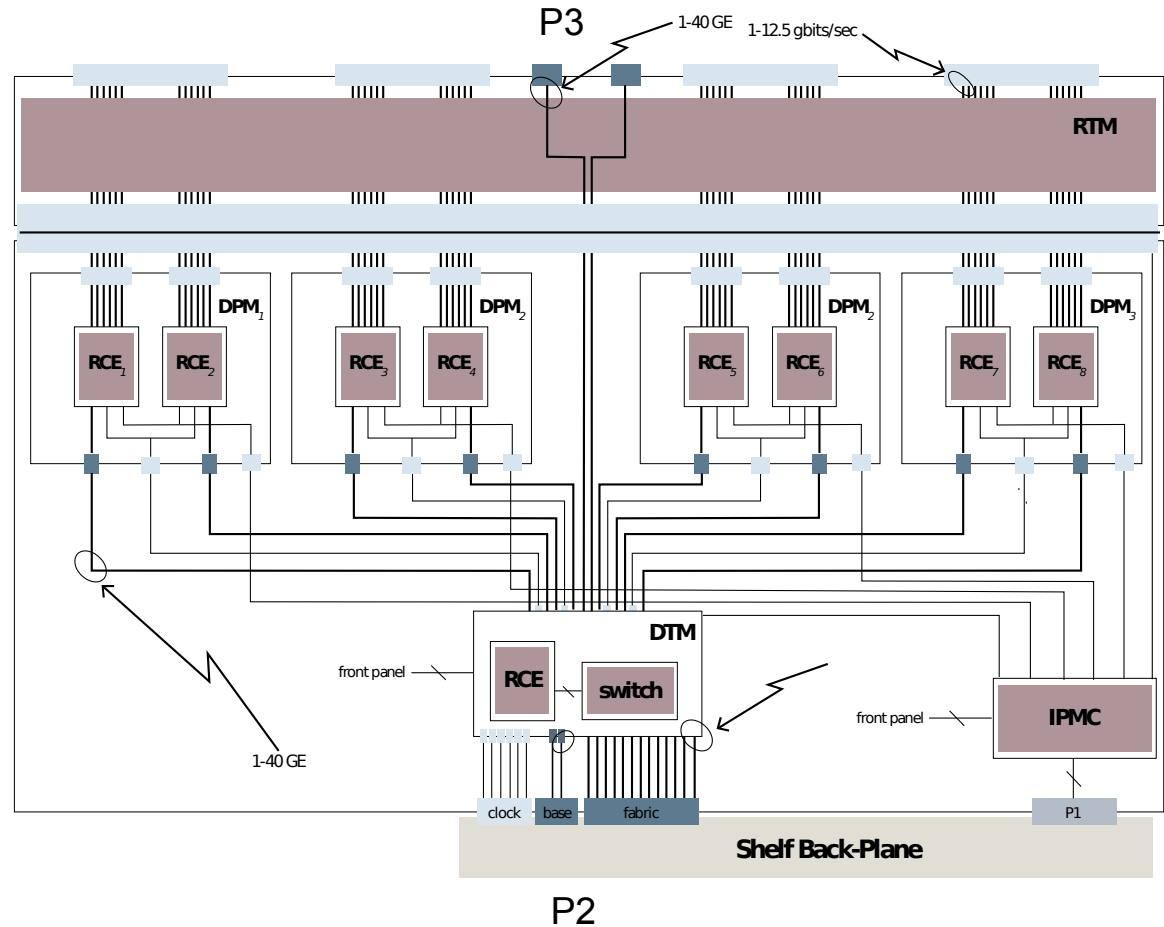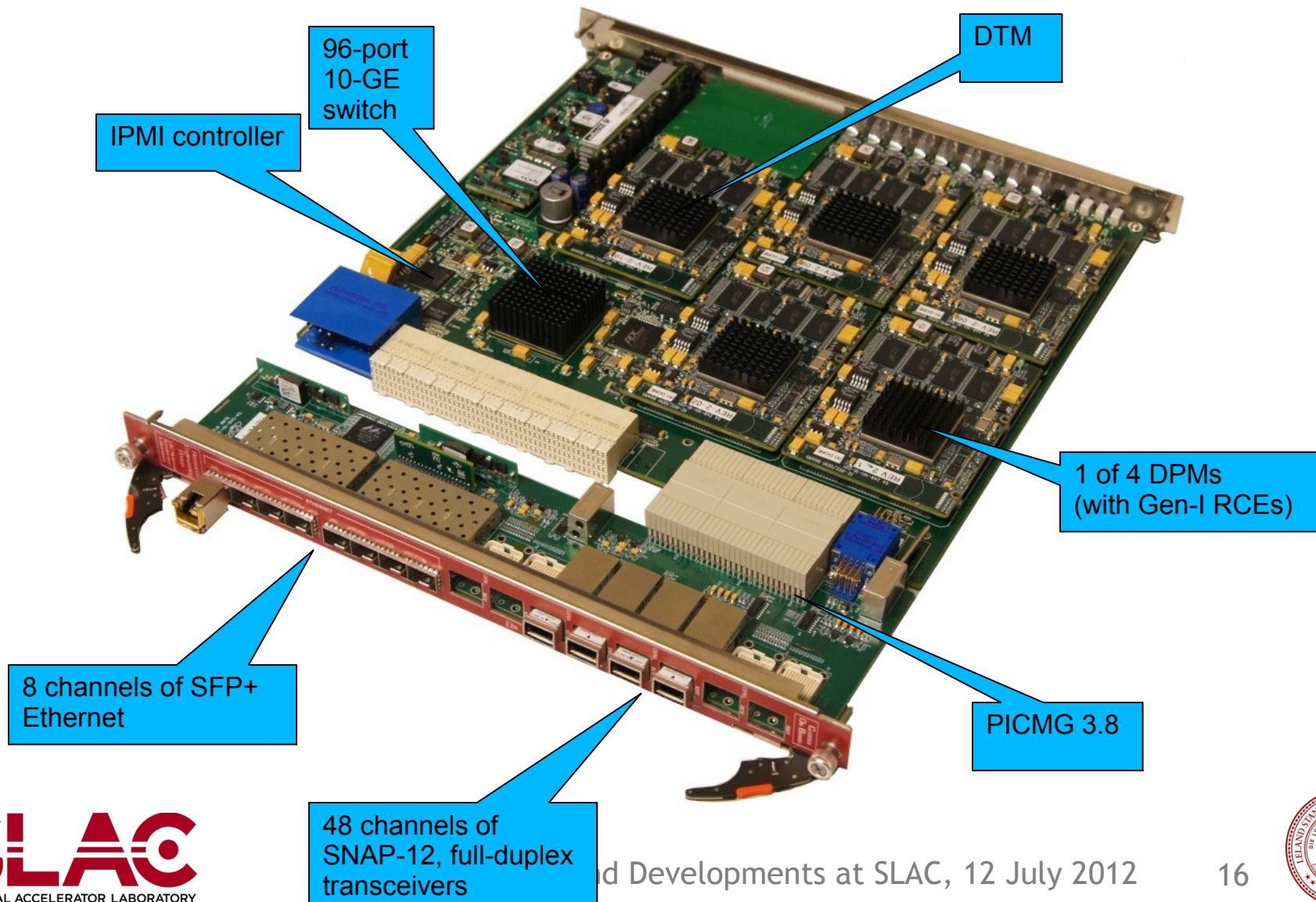
SD configuration flash

4 GBytes (DDR3)

SOC

Cluster On Board (COB)

- 4 Data Processing Modules (DPM)
  - » Dual RCE (6 MGT), or
  - » Single RCE (6 MGT), or
  - » Single RCE (30 slow I/O ports)
- 1 Data Transport Module (DTM)
  - » 1 control RCE
  - » 24 port x 40GE switching capacity
  - » 2x40Gb/s Ethernet port
  - » Front TTC interface (FTM)
- Rear Transition Module (RTM)
  - » User interface via P3

COB + 48 channel R/O + 80 Gbits/s Ethernet RTM

96-port 10-GE switch

IPMI controller

DTM

1 of 4 DPMs (with Gen-I RCEs)

8 channels of SFP+ Ethernet

48 channels of SNAP-12, full-duplex transceivers

PICMG 3.8

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Applications outside ATLAS

- **Large Synoptic Survey Telescope (LSST)**
  - » 3.2 billion pixel camera
  - » 12.8 Gbytes every 39 s (330 MB/s sustained)

Cerro Pachón – Future site of the LSST
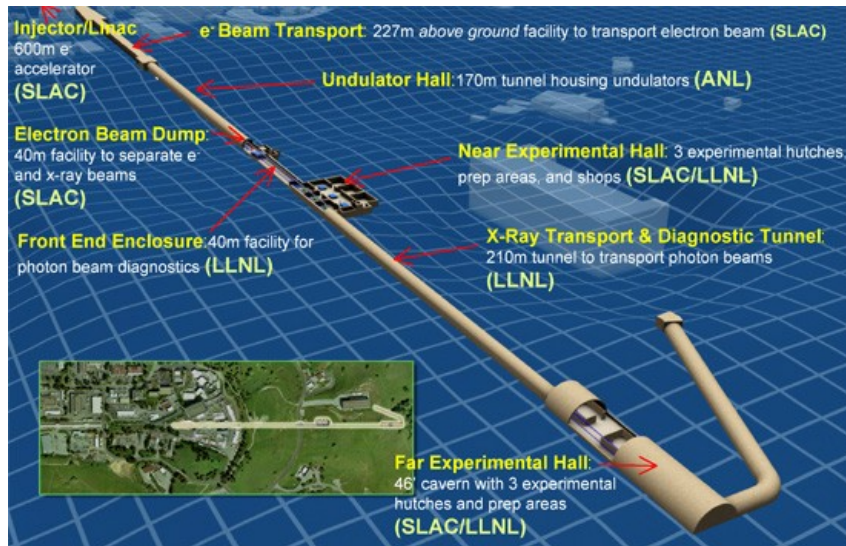
- **LINAC Coherent Light Source (LCLS)**
  - » X-ray free electron laser, femtosecond pulses
  - » Variety of experiments and read-out

Applications of RCE/ATCA to ATLAS Pixel

- Full suite of pixel calibration code runs on new readout ASIC FE-I4 for IBL. The same setup/software runs from single chip test stand to full system

- Running ATLAS TDAQ software on RCE under RTEMS

- IBL stave-0 test setup at CERN

- Running test beam setups with EUDET/TimePix at 15 kHz
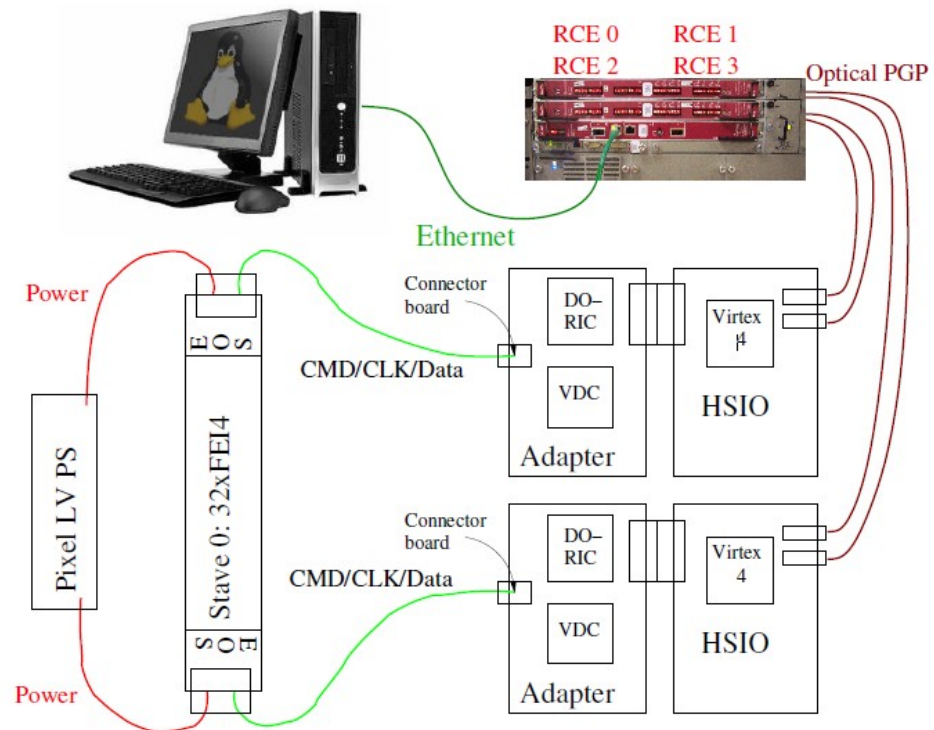
Status and Plans (I)

- Program Status:
  - » Phase-I complete
  - » Phase-II scheduled to complete ~ last quarter this calendar year
  - » Phase-III after that
- Deployed currently:
  - » For the LCLS experiment detector readout DAQ
  - » For the Heavy Photon Search test-beam DAQ
  - » As readout technology for IBL stave testing (for example CERN's SR1 & U Geneva IBL stave loading site)
  - » For the pixel planar sensor test beam readout
  - » As the test-stand for LSST Camera CCD read-out

Status and plans (II)

- Chosen as the core technology for:
  - » The LSST camera's DAQ system
  - » The alternative final readout scheme for IBL as well as the AFP (ATLAS Forward Physics) silicon detector readout
  - » The pixel beam telescope readout for an upcoming SLAC test beam
  - » The ATLAS CSC ROD replacement in 2014
  - » The AFP timing detector readout for 2014
- Candidate technology for:
  - » The Readout replacement (ROD) of the SCT in 2014
  - » The New (Muon) Small Wheel readout for the ATLAS Phase-1 upgrade (2018)
  - » The Silicon tracking upgrade (both strip & pixel) readout for ATLAS Phase-1 & Phase-2 upgrades
  - » The Readout systems of the (D3) Directional Dark matter search Detector proposal from U Hawaii
  - » The DAQ system of the LBNE (Long Baseline Neutrino Experiment) far detector

DAQ Development Timeline – Project Specific Applications

Future generic R&D funded

E.g. improving current version, porting from *INTEL* "Tahoe" family to the *INTEL* "Alta" family, porting to ARM architecture, next generation switch and FPGA

Proposed

Silicon tracker upgrade (both strip and pixel) readout for the ATLAS Phase-1 (2018) and Phase-2 upgrades (2021)

New (Muon) Small Wheel readout for the ATLAS Phase-1 upgrade (2018)

LBNE far detector DAQ system

Potential readout replacement of the SCT in 2014

Decided on

LSST DAQ

ATLAS CSC ROD replacement in 2014

Pixel beam telescope readout for upcoming SLAC test beam

AFP timing detector project for 2014

Employed

HPS testbeam

LSST string-test

Pixel planar sensor testbeam readout

PETA Cache

LCLS
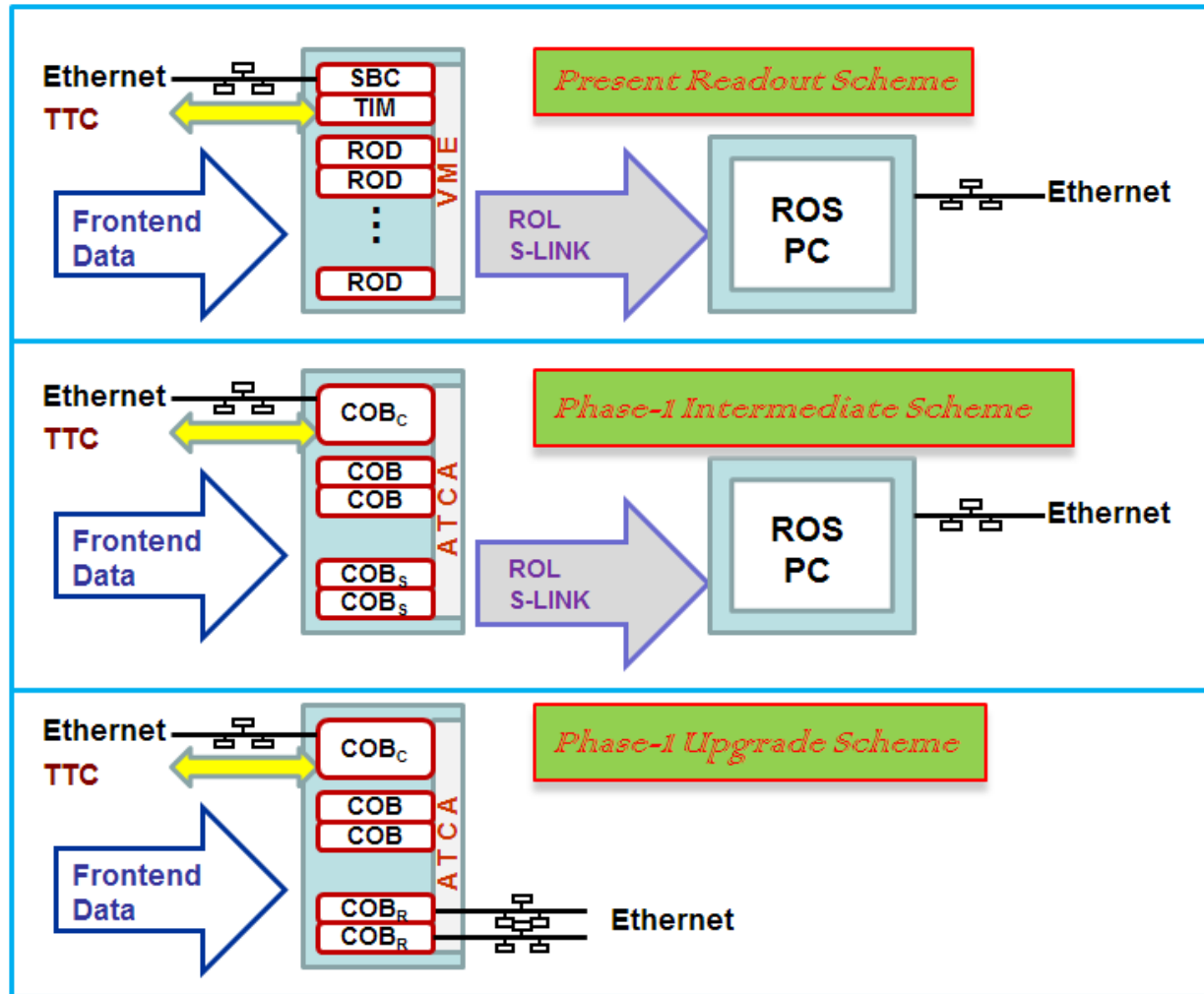
CERN IBL module testing at several sites

Project funded   **Past generic R&D funded**   **Project funded**

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Architechtural Possibilities with ATCA

Answers to some of the questions

- What is the expected usage of the backplane?
  - » 10 GE ethernet and TTC.
- Would you agree for a control through Ethernet?
  - » Yes.
- Do you use synchronisation signals and common clocks?
  - » Yes, any system, but we are adding TTC.
- Do you plan to use redundancy and/or hot swapping?
  - » No, but it is possible.
- Do you plan full mesh or dual star backplane?
  - » Either. Full mesh is (by far) preferred.
- Typical expected power consumption?
  - » 70W – 100W / front board. RTM is application specific.
- Which crate size to you plan to use (i.e. how many slots available)?
  - » Don't care (application specific).
- Do you plan implementation with AMC mezzanine and a mother board?
  - » No.
- How sure are you you need ATCA. Could you envisage μTCA?
  - » Need ATCA.
- Do you need zero, one or more ATCA switch blades in your ATCA shelf? Which kind of switch?
  - » None (built into our front board).

Summary

- SLAC has been using ATCA since 2007, in particular for the generic DAQ components developed by Mike Huffer *et al.*

- ATCA-based DAQ has been deployed at the Linac Coherent Light Source and in test beams at various sites including CERN, and is the chosen technology for the Large Synoptic Survey Telescope and other applications

- In ATLAS, ATCA is already in use for IBL stave testing, planar pixel test beam read-out

- ATCA-based systems will be deployed as
  - » CSC RODs after LS1
  - » AFP timing detector

- ATCA DAQ is being proposed and considered for IBL, SCT, New (Muon) Small Wheel

Conclusions

- The decision 5 years ago to leverage the ATCA industry standard proved as an excellent decision

- At the technical level, our basic recommendations are simply:
  - » Radial rather than bussed IPMB
  - » Full mesh rather than dual star

THANKS!