Minutes of the Calorimeter Upgrade Meeting

CERN, February 17th, 2012

1 Introduction (Frédéric)

- An addendum to the LOI should be written by end of May. It concerns mainly the costs and commitments. The members of the group should try to clarify the expected costs and try to see how the actual commitments should be confirmed by the instituts. The phase (R&D, production,...) to define the costs and commitments is not clear and a mail was sent to Andreas in order to clarify this. It seems by far not feasible to have a firm engagement of the instituts for the production before the LOI addendum deadline.
- The url for the calorimeter upgrade pages is now
  https://twiki.cern.ch/twiki/bin/view/LHCb/CaloUpgrade
- Common tests at Barcelona are planned for the three day period of March 19th, 20th and 21st.A tested digital board from LAL should be brought to Barcelona for the test.
- Still a few tasks are not covered
  - SPD/PRS studies → **very problematic**
  - Control board development
  - Design of the optical GBT mezzanine
  - Firmware development
- 2 Monte Carlo samples for SPD/PRS studies have been produced in the upgrade conditions : luminosity=$2x10^{33}cm^{-2}.s^{-2}$, E=14TeV, cross-section ~102mb, crossing rate ~30MHz and for the event type $B \rightarrow K^* \gamma$. The detector is either equivalent to MC11a or MC11a with SPD/PRS/Lead removed. Details can be found on the calorimeter upgrade pages.

2 Analog Electronics session

Discrete component design (Carlos)

- Many tests have been performed on the analog electronics (discrete components).
- Most of the problems which had been identified at a earlier stage of the development have been solved (the integrator does not oscillate any more). The AO AD4A932 (amplification) (ADA4938 for clipping, integration) is now used and offers a x2 dynamics with respect to ADA4930. No problem is seen with this OA, but radiation tests should be done to fully validate it.
- The amplifying and clipping stages have been tuned from simulation studies. The question was asked on the reliability of the simultation to estimate the best parameter for the adjustments.
- With those parameters the behavior of the system is satisfactory
  - the plateau width is of the order of 5ns,
  - the linearity has to be properly determine but is most certainly better that the specs and lower than 1%

The only worry concerns the width of the integrated pulse which is larger than 50ns and leads to a spill over of more than 4%. It was asked whether a tuning of the RC of the integrator or of the clipping could solve this without affecting too much the plateau (defined by a 1% variation) width.

- Noise has been measured in different conditions :
  - Anechoic chamber : no difference wrt “default” → the design seems to be immune
  - Connecting a “PMT” cable at the input
  - Joining or not the ground of the analog and digital parts
  - etc...

It seems that the noise increases when a “PMT” cable is connecting only in the joined ground case. The pedestal subtraction does not solve the problem and it seems the effect is linked to a high frequency noise. The cause for this noise and the interplay with the joint grounding is not clear.

It was also mentioned that a 10MHz synchronous signal should be generated by the LAL digital board in order to reduce jitter problem in generating input pulses. Should see whether the divided clock is usable here.

ASIC design (David)

- Several measurements have been presented
- The linearity has been measured on several chips and channels. The results are coherent and within specs.
- The plateau width is also satisfactory (~5ns for 1%).

3 Digital session

Status of the firmware (Olivier)

- Two aspects of the digital electronics have been presented :
  - the acquisition part is ready for the common tests planned in March
  - the second aspect concerns the test of the A3PE and its ability to run at high speed with many IOs.The firmware has been written and is being tested. The tests have been stopped recently because of problems in the loading of the firmware of the FPGA. Olivier and Thierry recently focused on this issue.
- It was emphasized that the second board which is at LAL should be debugged and upgraded. This would be a backup solution if FPGA firmware loading is still problematic on the first mother board.

4 Preliminary results from the module irradiations (Yuri)

- Yuri sent a few slides with preliminary results on the response of the modules which have been stored close to the beam in the LHC tunnel and that received from 100 to 200krad.
- The passive dosimeters have been removed to be readout and to obtain a better estimation of the dose received..
- The results have been compared to another module which has received ~2Mrad in a particle beam.
  - The 2 modules of the tunnel do not show any damage.

- The highly irradiated module shows on the contrary an important effect which looks in agreement with the results obtained last year. This seems to confirm that the modules of the calorimeter will have to be replaced if we want to be in specs for the upgrade runs.
- The shape of the response of the modules along the z-axis and for the highly irradiated module seems to indicate that the dammaged part is not the fiber but rather the plastic (a slope in the attenuation of the signal is not observed along z)..

5 Discussion on ECS

- Cyril expressed the possibility to emulate the GBT-SCA in the TVB Glue. This would require enough lines on the backplane between the control board and the TVB (glue component) to propagate the e-links. This should be looked at by Cyril. Kostas should also be contacted to know the portability of the GBT-SCA in the Actel ProAsic.

- The present electric standard for the IOs of the GBT-SCA are a bit problematic. We would like to be able to use 3.3V IOs especially for the ICECAL ASIC. A survey in the collaboration should be done by Ken to see if this is a general requirement. Then, we may ask GBT designers to implement 3.3V IOs. 2.5V should be OK for the GBT designer (no radiation problem that could appear for 3.3V) but this is still not easy for the ASIC (digital standard cells and IO pads characterized for 3.3V operation only).